Quasi-Static Energy Recovery Logic and Supply-Clock Generation Circuits

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Abstract

A Quasi-Static Energy Recovery Logic family (QSERL) using two complementary sinusoidal supply clocks is proposed in this paper. A high-efficiency clock generation circuitry which generates two complementary sinusoidal clocks required by QSERL is also presented. The clock circuitry locks both frequency and phase of clock signals, which makes it possible to integrate adiabatic module into a VLSI system.

We have designed an 8x8 carry-save multiplier using QSERL logic and two phase sinusoidal clocks. SPICE simulation shows that the QSERL multiplier can save 37% of energy over static CMOS multiplier at 100 MHz.

1 Introduction

Numerous designs of adiabatic logic have been presented in [1, 3, 4, 5, 6, 7, 8], demonstrating the possibility of achieving low energy computing. We propose a Quasi-Static Energy Recovery Logic (QSERL) which uses two complementary sinusoidal supply clocks and possesses several positive characteristics of static CMOS logic. Circuit nodes are not necessarily charging and discharging every clock cycle in QSERL, which reduce the node switching activities significantly. The lower switching activity reduces energy dissipation. A preliminary version of QSERL was introduced by authors in [6] and by De in [9]. The QSERL presented in this paper has been modified for complex gates. We also present an alternative approach which eliminates diodes by using augmented circuitry.

A high-efficiency clock generation circuitry which generates two complementary sinusoidal clocks required by QSERL circuits is also presented in this paper. The adiabatic clock circuitry locks both frequency and phase of the clock signals, which makes it possible to integrate the adiabatic module into a VLSI system.

We have designed and simulated an 8x8 carry-save multiplier using QSERL. Results are also compared to a static-CMOS carry-save multiplier.

2 Quasi-Static Energy Recovery Logic

Fig. 1 shows a schematic of QSERL which resembles the static-CMOS logic with two additional diodes for each gate. The diode on the top of the p-mos tree controls the charging path, while the other diode at the bottom of the n-mos tree controls the discharging path. Two sinusoidal clocks in complementary phases, \( \Phi \) and \( \bar{\Phi} \), are sufficient. Note that cascaded gates are in alternate phases. The second gate in Fig. 1 evaluates its logic value while the first gate is in hold phase. For the basic operation of QSERL logic, readers are referred to [6] and [9]. In contrast to dynamic adiabatic logic in which each gate charges and discharges in every cycle, QSERL is "static". Circuit nodes are not necessarily charging and discharging every clock cycle, reducing the node switching activity substantially.

The diodes used in QSERL for controlling the charging and discharging paths can be replaced by low-threshold voltage MOSFETs. There are three possible ways to connect the diodes as shown in Fig. 2. We use the connection shown in Fig. 2(c) due to the following reason: The voltage drop \( V_{PS} - V_{NS} \) across the p-mos tree when charging (and \( V_{NS} - V_{PS} \) across the n-mos tree when discharging) results in larger gate-to-source voltage \( V_{gs} = V_{GS} - V_{PS} \) for \( P_d \) and \( V_{gs} = V_{GS} - V_{NS} \) for \( N_d \). Hence, with the diode configuration of Fig. 2(c), the voltage drop in the charging/discharging path makes the diode MOSFETS \( P_d \) and \( N_d \) stronger in conduction.

Since \( P_d \) and \( N_d \) function as diodes, the energy dissipation at \( P_d \) (\( N_d \)) for charging (discharging) a circuit node is \( CV_{t} (V_{dd} - V_{t}) \). Hence, it is essential to reduce the threshold voltage of the control transistors \( P_d \) and \( N_d \) for lower power dissipation. However, circuit nodes are floating in some portion of a clock cycle. The larger leakage current due to lower threshold voltage can cause more noise. Simulation indicates that it is safe to lower \( |V_{t}| \) of both p-mos and n-mos devices to 0.2 volt when frequency \( f \) > 10 MHz at 3.3 volt supply voltage.

We simulated an 8-inverter chain implemented using QSERL logic of Fig. 2(c) and QSERL with ideal Schottky diodes (threshold voltage \( \approx 0.3 \) volt) respectively. 0.01pF of internal capacitance (wiring, interconnection, etc.) is assumed at the output node of each inverter. Results are sum-
Quasi-static Adiabatic Multiplier

We have designed and simulated several QSERL circuits. In this section, we address some issues we observed in designing QSERL circuits. Design and simulation results of an 8x8 QSERL multiplier will also be explained.

3.1 Noise reduction for complex gates

The output node of a QSERL gate is floating in half of a clock cycle (in hold phase) which introduces noise. We observed that this noise is usually tolerable for two input logic gates. When implementing a complex function into one gate, noise may cause incorrect operations, especially at high speed. For circuits such as multiplier which consists of an array of adders, a mixed approach – mixing conventional CMOS and QSERL logic may be a good choice to keep the noise to minimum. Let us consider a complex gate in Fig. 4(a). A clocked inverter loop is used to keep the output signal constant in hold phase. CL is a conventional pulse clock signal which is HIGH when Φ is in hold phase and is LOW when Φ is in evaluation phase. Thus, the inverter loop is ON in hold phase and keeps the output node at constant voltage level. The integration of adiabatic gates and standard CMOS circuits is ensured by the supply clock generation scheme given in Sec. 4, in which the supply clock is synchronized to the reference clock. Minimum size transistors can be used for P1, P2 and N3, N1 should have larger size to force the inverter loop to settle to its state fast. In contrast, P1 can have minimum size since it is not clocked. For a full adder, 10 transistors are needed to generate the carry and 14 transistors for the sum. Many transistors are fairly large because of large fan-out (10 for carry) in a carry-save multiplier. Hence, the energy consumed in P2, N2, and clock signals is still a small portion for a complex gate.

When differential signaling is used (often preferred in arithmetic circuits), it is simpler to implement the noise-reduction inverter loop. Let us take a 3-input XOR gate of Fig. 5 as an example. Both sum and carry are available, thus a pair of cross coupled inverters will lock the outputs in hold phase (Fig. 5(b)). Minimum size transistors can be used in the two inverters.

3.2 Elimination of diodes in QSERL logic

Diodes can be avoided if we put an extra latch as shown in Fig. 4(b). The diodes D1 and D2 can be replaced by Pa and Na, respectively. The output y of the latch has the same value as the gate output signal x. This signal will be at the output of the latch in the next clock cycle, i.e., y will remain unchanged in the next evaluation phase. If the gate output x is LOW in the current cycle, then y is LOW in the next evaluation phase. Hence Pa is turned ON and Na is turned OFF. The gate is ready for charging to high if a
path in p-mos tree is ON. Conversely, if $x$ is HIGH in the current cycle, then $N_a$ is turned ON and $P_a$ is turned OFF in the next evaluation phase.

### 3.3 An 8x8 QSERL multiplier

We have designed an 8 by 8 carry-save adiabatic multiplier using QSERL logic and two-phase sinusoidal supply clock. The adder cell is implemented using 3-input XOR gate shown in Fig. 5. The last stage of the multiplier is a 7-bit carry-lookahead adder.

The multiplier was simulated using MOSIS 0.5 μm CMOS NWELL process. The transistors functioning as diodes need to be sized up as the frequency goes higher. The rest of the n-mos transistors are of size $l/w = 3 \lambda / 2 \lambda$ and p-mos transistors are of size $l/w = 6 \lambda / 2 \lambda$, where $\lambda = 0.3 \mu m$. Results are compared to a static CMOS carry-save multiplier using the same transistor size. Simulation was performed using 64 randomly generated input vectors which are independent with each other. The probability of being HIGH (and LOW) for each input in each clock cycle is 0.5, and the probability that an input switches in the following cycle is also 0.5. Fig. 6 shows the energy consumption per clock cycle for the 8x8 QSERL multiplier and static-CMOS multiplier. The adiabatic circuits exhibit significant energy savings. At 10 MHz the energy saving is more than 50%, and at 100 MHz the energy saving is 37%. At 200 MHz, there is only 8% energy savings for the adiabatic multiplier.

While adiabatic circuits maintain reasonably high throughput, the input/output latency is large. Our 8x8 QSERL multiplier has a latency of 12 clock phases (6 clock cycles). Hence, it seems that adiabatic technology is more suitable for some specific applications where speed and latency are not critical.

### 4 Supply Clock Generation Circuit

Research on design of highly efficient resonant drivers for generating adiabatic supply clocks has started in earnest [2, 4, 5]. So far, the frequency range for the existing schemes is fairly low (well below 100 MHz), prohibiting its use in high frequency environment. In addition, the existing schemes work in a frequency determined by inductor(s) and the capacitive load rather than the external frequency. Hence it is not possible to integrate the adiabatic module into a VLSI system in which the rest of the system operates in a frequency defined by the system.

Fig. 7 shows the resonant driver we proposed for generating adiabatic supply clocks. The oscillator generates two complementary phases of nearly sinusoidal waveforms. Two p-mos transistors ($P_1$ and $P_2$) and two n-mos transistors ($N_1$ and $N_2$) are used for energy replenishment and frequency-phase lock-up. The circuitry starts to oscillate when the control signal $enable = 1$ and cease to oscillate when $enable = 0$ (because the pull-down transistors $N_1$ and $N_2$ are turned ON and the pull-up transistors $P_1$ and $P_2$ are turned OFF). The size of these four transistors are determined by the frequency it operates and the capacitive loads the circuitry is driving. The higher the frequency and/or the larger the capacitive load is, the larger size of the transistors should be so that a peak operating voltage $V_{dd}$ is achieved. The optimal size can be found by simulations. Unlike the previous scheme [2], no reference voltage source is needed. There is no serial connected transistor in the driver circuitry, hence the energy efficiency is mainly determined by the load, i.e., the resistance $R$ in the clock distribution lines and the capacitive load $C$. One inductor is sufficient. The value of the inductor is determined by resonant condition at the given frequency. Simulation results indicated that $L$ should be slightly larger than the theoretically calculated value for optimal efficiency. The PLL samples the clock signal(s) at the load and produces two control signals $C_1$ and $C_2$ at frequency of the ref-
ference clock, which in turn forces the circuitry to oscillate at the frequency of the reference clock. The two control signals \( C_1 \) and \( C_2 \) are 180 degrees out of phase, each of which is a pulse signal with 25% duty cycle only (the duration that the signal is HIGH is 25% of a clock cycle). The transistors of the inverters (INV1, INV2), NAND gates (NAND1, NAND2), and NOR gates (NOR1, NOR2), which are controlling the replenishing transistors, should be much smaller than the replenishing transistors (e.g., approximately 1/20 of the replenishing transistors at 100 MHz). Thus, the voltage at the gate of a replenishing transistor has finite rise and fall time. Approximately a triangular waveform is produced at the gate of each replenishing transistor. The optimal rise and fall time should be close to 25% of a clock cycle such that each replenishing transistor is ON for approximately 50% of the time. The replenishing transistors turn ON and OFF gradually so that only small interferences are imposed on resonant circuitry, which ensures that the waveforms at both sides of the inductor are nearly sinusoidal. Sinusoidal waveforms have the highest energy efficiency as energy for the higher order harmonic components are nearly completely dissipated in the resistances of clock distribution lines and resistive loads. The p-mos and n-mos replenishing transistors on one side (e.g., \( P_1 \) and \( N_1 \)) never turn ON simultaneously to prevent the short circuit current. All transistors in the control gates (INV1, INV2, NAND1, etc.) are small. The energy consumed in these control gates is negligible.

Fig. 8 shows the waveforms of a control signal \( C_1 \) from PLL (top of Fig. 8), voltage at the gate of the replenishing transistors \( P_1 \) and \( N_1 \) (middle of Fig. 8), and the clock waveforms produced at the output (bottom of Fig. 8).

We define the energy efficiency of the supply clock generation as the ratio of energy delivered from DC (equals to the energy dissipated) and \( CV^2 \), where \( V \) is the peak voltage. The replenishing transistors are sized to satisfy \( V_{\text{peak}} \approx V_{\text{dd}} \).

Fig. 9 shows the energy efficiency of our scheme, which is obtained from simulations for \( R = R_2 = 50 \Omega \) and \( C = C_1 + C_2 = 100 \mu F \). The energy efficiency is approximately 95% at 100 MHz for the chosen \( R \) and \( C \) value. It is essential to minimize \( R \) in the supply clock distribution network to obtain high energy efficiency. Since supply clocks replace power lines, the resistance is sufficiently low. When the load capacitances are excessively large, multiple clock generation circuits connected in parallel are needed to have high energy efficiency.

5 Conclusions

In this paper, we presented QSERL, a low-energy, quasi-static adiabatic logic family. QSERL has lower switching activity than dynamic adiabatic logic and possesses several positive characteristics of static CMOS.

A scheme to generate two complementary sinusoidal supply clocks for QSERL circuits is also presented. The circuit can lock the supply-clock frequency to the system clock, and hence makes it possible to integrate QSERL circuits into a conventional VLSI system.

REFERENCES


Figure 8: Waveforms of the resonant driver.

Figure 9: Energy efficiency of the adiabatic clock generation circuitry.