High-Performance, Low-Power Design Techniques for Dynamic to Static Logic Interface

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Abstract
To optimize performance and power of a processor with both precharged and static circuit styles, a self-timed modified cascode latch (MCL) is proposed for dual-rail domino to static logic interface. Compared to conventional self-timed cascode and cross-coupled NAND latches, the innovative MCL achieves the highest performance and lowest power dissipation with reasonable noise immunity. Ease of embedding logic functions in these self-timed latches is also studied. For interfacing single-rail domino to static logic, the pseudo-inverter latch (PIL) is the most power efficient latch when compared with the conventional transparent and cross-coupled NAND latches. Based on a 0.18 μm CMOS nominal process with a 1.6 V supply voltage, effects on these latches' power dissipation and delay from scaling supply voltage and output load are presented, respectively.

I. Introduction
Dynamic logic has been known to achieve higher performance than static logic [1] at the expense of higher design risks. Such design risks include noise immunity, charge sharing, substrate charge injection, cross-talk, and power dissipation [2] [3]. As the processor clock frequency continues to increase, one approach to balance the design risk with the demand for higher circuit performance is to apply dynamic logic in speed-critical area only. Hence, an efficient interface scheme between dynamic and static logic is needed for high-speed designs with both circuit styles.

In this paper, we present a study of dynamic to static latch interface. First, speed, area, power dissipation, and noise immunity of three data-driven, self-timed latches that interface dual-rail domino to static logic are investigated: a cascode latch, a cross-coupled NAND latch, and the proposed modified cascode latch (MCL). Then, the discussion is extended to address delay and power of three clock-driven latches that interface single-rail domino to static logic: a conventional transparent latch, a cross-coupled NAND latch, and the pseudo-inverter latch (PIL). The analysis is performed based on a 0.18 μm CMOS nominal process, 1.6 V supply, 25°C temperature, and 100 MHz clock frequency.

II. Dual-Rail Dynamic to Static Latches
In this section, three data-driven, self-timed latching techniques interfacing dual-rail domino to static logic are investigated. Results of the analysis are presented with respect to delay, power dissipation, area, and noise immunity.

2.1 Cascade Latch
A self-timed cascode latch [4] is illustrated in Fig. 1a. The latch inputs are driven by the inverters of the preceding dual-rail dynamic gates. During the precharge phase, signals IN_L and IN_H are at logic-0, nFETs N1–N4 are switched off and the state is stored in the cross-coupled inverters. When the evaluation phase starts, assuming IN_L is 1 and IN_H is 0, N2 and N4 are turned on to form a push-pull force on the cross-coupled inverters. Since ZZ_L is pulled high by N4, the nFET body effect slows down the rising edge of the signal. The pFETs of the cross-coupled inverters needs to be sized large enough to pull the ZZ node to Vdd promptly to minimize short-circuit power dissipation. The nFETs of the cross-coupled inverters are minimum size transistors. The Wp/Wn ratio of the output inverters is set to 1 to compensate for the slow rising edge on the ZZ nodes.

2.2 Cross-Coupled NAND Latch
A cross-coupled NAND latch is shown in Fig. 1b. During the precharge phase, signals IN_L and IN_H are at logic-1. The cross-coupled NANDs behave like a pair of cross-coupled inverters to keep the state. During the evaluation phase, assuming IN_L is at
logic-1 and \( \text{IN}_L \) is at logic-0, it forces \( \text{OUT}_L \) to logic-1 and \( \text{OUT}_H \) to logic-0.

2.3 Modified Cascade Latch (MCL)

To improve the slow rising edge of the ZZ nodes in the cascode latch, a modified cascode latch (MCL) is proposed (Fig. 1c). It replaces the nFETs \( N1 \) and \( N4 \) of the cascode latch with two pFETs, \( P1 \) and \( P4 \). The inputs to these pFETs are the dynamic nodes of the preceding dynamic gates. During the precharge phase, \( \text{IN}_L \) and \( \text{IN}_H \) are actively driven high by the precharge pFETs to switch off \( P1 \), \( P4 \), \( N2 \), and \( N3 \), while the ZZ nodes maintain the state. During the evaluation phase, \( \text{IN}_L \) and \( \text{IN}_H \) are in the pseudo-dynamic state driven by either the cross-coupled pFETs (much stronger than the feedback pFET of the single rail dynamic logic) or the N-network. The ZZ nodes in the MCL are actively driven by either \( N2-P4 \) or \( N3-P1 \) pair. Since the pFETs \( P1 \) and \( P4 \) do not have the pull-up problem as the nFETs \( N1 \) and \( N4 \) of the cascode latch, the cross-coupled inverters in the MCL are minimum size gates. The rising edge of the MCL output is slower than the falling edge due to one extra inverter gate delay (Fig. 1c). Thus the input and output inverters are sized to a 3:1 \( W_p/W_n \) ratio.

2.4 Delay Comparison

When comparing the speed of the three self-timed latches discussed above, a 3-input dual-rail domino XOR was used as the driving gate, and a 0.3pf capacitor was used as the output load. Each latch was then sized to achieve its best performance. Delays were measured from clock rising edge to outputs in order to comprehend input loading effect of the latches. As shown in Table 1, the MCL is the fastest latch. It is 26% faster than the cascode latch because it has one less gate to traverse to the output falling edge. In addition, the pFET pull-up on the ZZ nodes of the MCL is faster than the nFET pull-up of the cascode latch. The cross-coupled NAND latch has a larger capacitive load to the preceding n-Network, thus, it is 27% slower than the MCL.

To further understand the drive characteristic, Fig. 2 illustrates the latch delay versus output loading. The MCL has the best performance. The cross-coupled NAND latch is faster than the cascode latch when the output load is 0.3pf or smaller. It becomes slower when the output load increases because the stacking nFETs of the NAND gate have larger channel resistance, hence weaker drive strength. One advantage of the cascode and MCL latches is the ease of embedding logic functions. The addition of NAND/AND functions to MCL (Fig. 3) costs only 20ps speed degradation. For the cascode latch, as the number of stacking nFETs increases with embedded functions, the pull-up strength of ZZ nodes degrades because of the increasing body effect, regardless of the nFET size. This speed penalty eventually offsets the advantage of embedding logic function in the cascode latch. It is difficult to embed functions into a cross-coupled NAND latch. The performance degradation of the functional (Fig 3b) cross-coupled NAND latch is 110ps, which is equivalent to a NAND gate delay time. Fig. 4 depicts the delay of the three functional latches with various output loads.

2.5 Power Dissipation Comparison

As shown in Table 1, the MCL dissipates 34% less power than the other two latches. It consumes less short-circuit power than the cascode latch. In addition, the MCL does not have the large stacking nFETs as the cross-coupled NAND latch, hence less capacitive power dissipation. Fig. 5 illustrates the power dissipation of the three self-timed latches with respect to \( V_{dd} \) scaling, and the MCL exhibits a lower power dissipation across the \( V_{dd} \) range compared.

2.6 Noise Immunity Comparison

The noise margin of the input nodes for each latch is summarized in Table 1. Noise can be characterized by its amplitude and pulse width. It has been shown that for a fixed input noise amplitude, the output glitch reaches a maximum value with a long input noise pulse width [5] [6]. In this analysis, noise margin is defined as the amplitude of the noise injected to the inputs that can switch the state of the latch, while assuming an infinite noise pulse width. The cascode latch has the best (1.01V, see Table 1) noise immunity on inputs among the three latches compared. It is harder to change the state of the cascode latch because of the weak nFET pull-up capability. Also, the inputs of the cascode latch are connected to the preceding dynamic gates’ output inverters, which make it less susceptible to noise. The inputs to the MCL need to be carefully controlled because they are connected to the dynamic nodes of the preceding domino gates. With an input noise margin of 0.86V (Table 1), normal design and layout precaution for the dynamic nodes should be sufficient to satisfy its input noise margin requirement. The cross-coupled NAND latch has a
slightly better noise margin than MCL on its inputs (0.91V), but it is more susceptible to noise on its outputs as the storage element is exposed directly to the output load. In addition to the noise on the inputs, noise can also be injected into the dynamic ZZ nodes of the cascode and MCL latches. It is measured that the noise margin on the ZZ nodes is 0.8V. Since the ZZ nodes are usually short wires that can be well controlled in the layout, this noise margin of half $V_{dd}$ is sufficient.

III. Single-Rail Dynamic to Static Latches

Three clock-driven, single-rail dynamic to static latches (Fig. 6) are investigated: a transparent latch, a single-rail cross-coupled NAND latch [4], and the pseudo-inverter latch (PIL).

3.1 Pseudo-Inverter Latch (PIL)

The PIL (Fig. 6d) is improved from the precharged N latch (Fig. 6c) [6] by adding an inverter to the output of the dynamic node. The added inverter is used to reduce noise susceptibility of the precharged latch at its input. It also provides one more gate delay to avoid possible race conditions in the precharge N latch. This race condition occurs because the pFET (Fig. 6c) is turned on the moment the precharged signal goes one $V_{tp}$ below $V_{dd}$ when the nFET is still conducting, hence the state can be precharged away. The PIL replaces the nFET pull-down of the precharge N latch with a pFET pull-up gated by the inverted clock signal $xclk$. This pFET pull-up is used to isolate the latch from precharging when the $xclk$ signal is high.

3.2 Delay Comparison

All three investigated latches require clock signals to fall no later than the precharge signal's falling edge to avoid the race condition where data in the latch is overwritten by precharge. The cross-coupled NAND latch requires the clock signal to rise at least two-gate (NAND) delay before the precharge signal, which presents $ZZ_H$ high, to achieve one gate delay from $IN$ to $OUT$. At the beginning of the evaluation phase, the early rising of the clock signal will default the outputs to low until the preceding dynamic gate starts evaluating. Therefore, the device sizes are skewed to optimize the output rising edge transition time. The cross-coupled NAND latch is the fastest (Table 2) with a delay of 276ps. It is not desirable for the cross-coupled NAND latch to drive a large output load, as the noise coupling to the output can potentially flip the state of the latch. The PIL has a delay of 299ps which is comparable to that of the NAND latch. It is 38% faster than the transparent latch (Fig. 6a) because the slow transmission gate in the transparent latch. When output load increases, the NAND latch does not perform as well as the other two latches due to its stacking nFETs (Fig. 7).

3.3 Power Dissipation Comparison

The PIL dissipates 18% less power than the NAND latch as it has 43% less transistor width (Table 2). The PIL also consumes 10% less power than the transparent latch. The transparent latch has a higher short-circuit power due to the slow edge rate on the $ZZ_H$ node caused by the transmission gate. Fig. 8 shows the power dissipation of these latches with respect to $V_{dd}$ scaling. The PIL dissipates the least power over the $V_{dd}$ range compared. It is also noticed that all three latches produce glitches if the output stays high. This glitch can increase spurious power dissipation as it propagates through static gates [8].

IV. Dual-Rail vs. Single-Rail Domino

In this section, noise characteristic of dual-rail and single-rail domino logic is investigated. Then, power-efficient applications of the MCL and PIL latches are discussed.

4.1 Noise Immunity Comparison

Single-rail domino gates typically have a weak feedback pFET at the dynamic node to reduce effects from charge-sharing, cross-talk and subthreshold leakage (Fig. 6). Though increasing pFET size enhances the noise immunity, it introduces more contention to the dynamic node, therefore slows down the speed. Dual-rail domino with feedback pFETs has the same issue. To improve both speed and noise immunity, this paper focuses on dual-rail domino with cross-coupled pFETs at the dynamic nodes (Fig. 1). During the precharge phase, the cross-coupled pFETs are both turned off. During the evaluation phase, only one of the two dynamic nodes discharges and switches on the associated pFET without contention. Therefore, a larger pFET size can increase the noise immunity of the cross-coupled dynamic nodes without speed degradation. Fig. 9 compares output glitch voltage of the single-rail and dual-rail logic. Coupling noise is injected into the dynamic node during the measurement. When the cross-coupled pFETs of the dual-rail domino and the feedback pFET of the single-
rail domino are both minimum size, their noise characteristics are similar. A 55% ratio of coupling capacitance to total node capacitance will introduce a 0.2V glitch at the output. If the cross-coupled pFETs are sized the same as the precharge pFETs, the noise margin is improved significantly. It now takes a 72% capacitance coupling ratio to introduce a 0.2V output glitch.

4.2 Low Power Applications

One way to reduce power dissipation is to minimize unnecessary signal transitions. A dynamic signal introduces additional power dissipation because it can have two transitions within a clock cycle. It is desirable to convert dynamic signals to glitch-free static signals before they propagate through heavy loads. The three dual-rail data-driven dynamic to static latches described produce glitch-free static outputs. On the other hand, all three clock-driven single-rail latches can have output glitches when their outputs stay at logic-1. Fig. 10 compares the overall power dissipation between the dual-rail MCL and single-rail PIL. When the output bus capacitance is low, the PIL dissipates less power. As the bus load increases, the power dissipation of the PIL increases due to spurious transitions. The PIL consumes more power than the MCL when the load is greater than 1 pf. Another application for the MCL is to combine it with a sense amplifier (Fig. 11). This structure is faster, smaller, and more power efficient than a sense amplifier followed by a cross-coupled NAND commonly used in memory design.

V. Conclusion

High-performance, low-power latches interfacing dynamic and static logic have been investigated for designs with mixed circuit styles. For dual-rail domino logic, the proposed MCL is 27% faster and dissipates 34% less power than the cascode and cross-couple NAND latches, based on the conditions of a nominal 0.18 µm CMOS process, 1.6 V supply voltage, and 25°C. In addition, the MCL occupies up to 47% less silicon area than the other two approaches compared. The noise margin of MCL is comparable to that of the cross-coupled NAND latch. The cascode latch exhibits the highest noise margin of 1.01V.

For interfacing from single-rail domino to static logic, the PIL is the most power-efficient among the three latches compared. The PIL dissipates 18% and 10% less power than the cross-coupled NAND and the conventional transparent latches, respectively. If the highest speed is needed, the cross-couple NAND latch is 7% faster than the PIL, but at an expense of 43% more area.

In selecting between dual-rail and single-rail domino logic, the investigation further suggests that dual-rail domino with strong cross-couple pFETs exhibits much better noise immunity than the single-rail domino as it increases the tolerance of the capacitance coupling ratio from 55% to 72% if a 0.2 V output glitch is used as the upper limit. If an application demands the output of a dynamic-to-static latch to drive a long bus line with heavy load (e.g., greater than 1.0 pf), the dual-rail MCL is preferred because its glitch-free output.

References


<table>
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<tr>
<th>TABLE I. Comparison of dual-rail self-timed latches</th>
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<tr>
<td>1.6V, 0.3pf loading, 3-input XOR logic</td>
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<tr>
<td>-----------------------------------------------</td>
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<tr>
<td>Total gate width percentage</td>
</tr>
<tr>
<td>Power (incl. XOR) percentage</td>
</tr>
<tr>
<td>Delay (incl. XOR) percentage</td>
</tr>
<tr>
<td>Noise Margin for IN</td>
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</tbody>
</table>
Fig. 1. Dual-rail dynamic to static Latches

Fig. 2. Latch delay vs. load capacitance

Fig. 3. Example of different functional latches

Fig. 4. Functional latch speed vs. load capacitance

Fig. 5. Dual-rail latch power vs. $V_{dd}$ scaling

**TABLE II. Comparison of single-rail latches**

<table>
<thead>
<tr>
<th></th>
<th>Transparent Latch</th>
<th>Cross coupled NAND Latch</th>
<th>Pseudo-Inverter Latch</th>
<th>Unit</th>
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<tr>
<td><strong>Total gate width</strong></td>
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<td>percentage</td>
<td>91</td>
<td>143</td>
<td>100</td>
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<td>0.153</td>
<td>mW</td>
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<td>percentage</td>
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<td>118</td>
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<td><strong>Delay (incl. XOR)</strong></td>
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<td>299</td>
<td>ps</td>
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<tr>
<td>percentage</td>
<td>138</td>
<td>93</td>
<td>100</td>
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Fig. 6. Single-rail dynamic to static latches

Fig. 7. Single-rail latch delay vs. load capacitance

Fig. 8. Single-rail latch power vs. $V_{dd}$ scaling

Fig. 9. Output glitch voltage vs. cap. coupling ratio

Fig. 10. Power dissipation vs. bus load

Fig. 11. A sense amp. edge-triggered latch