Minimizing Power Dissipation of Cellular Phones

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Abstract

Power dissipation can be addressed at three different levels: system, architecture, and circuit. The system has to be designed to allow for efficient paging to allow the phone to sleep for long periods, and the access scheme and modulation method have a large impact on circuit performance. A proper architecture and circuit partitioning has to be chosen: off-chip devices offer lower current consumption, but signal routing may require high power levels. At the circuit level, optimized supply voltages and power-down modes are important for digital circuits. Dynamic-bias analog circuits may adapt to the signal and interference situation.

1. Introduction

Today’s cellular phones have become very popular because they offer a highly demanded service, mobile communication, in a convenient way. The power consumption of the phone is a vital parameter, as too-frequent charging or too-heavy batteries make the phone awkward to use. A typical GSM phone may be used for several days without recharging, even with the smaller batteries. In stand-by mode, a GSM phone may consume much less than 10 mA, corresponding to more than 50 hours of operation from a small battery. Talk-mode current consumption is much higher, some 200 mA, yielding perhaps 3 hours of talk time. Often it is, however, hard to give accurate numbers, or even compare different phones, because several use- and operator-related parameters control the average current drain. For example, the actual mix of stand-by and talk time, paging interval (typically 1–2 seconds), average range to the base station (which sets the antenna average power level, ≤ 0.25 W), and battery capacity have a strong impact on the charging interval.

2. Power-consumption distribution

In talk mode the current consumption is dominated by the power amplifier. For a typical GSM hand-set, the pulsed antenna power is 2 W with a duty cycle of 1/8 [1]. Due to losses in the antenna switch, duplexer, and matching network, the power amplifier (PA) has to deliver close to 4 W. Adding a PA efficiency of some 60% we get around 200 mA of current drain with a 4 V battery or 270 mA with a 3 V battery (assuming the PA runs off an unregulated voltage).

The non-PA parts of the RF circuitry may consume 10% of the PA current, or some 25–50 mA. The base-band circuits may also use a similar amount of current.

In stand-by mode, the current consumption is dominated by the receive circuitry (RF and base band) when the phone is listening for paging signals (page-scan mode). In the sleep-mode periods between page scans, clocks and timers dominate the current consumption. In addition to the radio circuits, display and SIM-card drivers may consume non-negligible amounts of current.

3. System-design issues

Often the hand-set designer has no choice other than to follow the system specifications. It is still, however, interesting to point out the power-consumption consequences of some system features.

The modulation scheme has a large impact on the PA power consumption. For example, GSM, DECT, and analog cellular systems like AMPS and NMT employ frequency modulation or continuous-phase modulation (CPM). These modulation types have constant envelope and the PA only has to amplify a carrier with varying phase; the amplitude is stable or varies very slowly. This allows the PA to be of class C: the power transistor is conducting less than one half cycle, resulting in a very high efficiency of some 60%.

In contrast to CPM, where only the phase angle varies, linear modulation schemes require both phase and amplitude variations. Because of the high carrier frequencies (1–2 GHz) it is difficult to make linear class-C amplifiers. Thus, linear modulation schemes, like the QPSK of the IS-95 narrow-band CDMA system, often require class-A amplifiers.

A class-A amplifier has a maximum efficiency of 50%, but reaches only some 40% in practice due to bond-wire losses.
and transistor saturation effects. Since the carrier envelope varies, the PA has to be designed for a higher output power than the average (possibly pulsed) output power. For QPSK, we have to add some 3 dB of PA power compared to a CPM signal of the same average antenna power. Thus, a QPSK PA will have roughly twice the current consumption, or \( 0.60 \times 0.40 / 2 \), of a CPM PA, which directly translates to shorter talk time. Linear, but yet efficient, power amplifiers is a very important research topic.

The QPSK modulation does, however, offer roughly twice the symbol rate for the same bandwidth and thus compensates for the higher PA current consumption by a higher data rate.

The IS-95 system has to use a linear modulation method because the received signals must look like noise, and signals from several units in the same band must add like noise. A CPM signal would not let the system behave properly as its information is in the phase only.

In addition to the modulation scheme, the duplexing method impacts the power consumption. If frequency-division duplexing (FDD) is used, the hand-set receive and transmit frequencies (RX and TX respectively) are separated by the duplexing distance. In, for example, the GSM system, the receive and transmit packages are separated in time (and frequency). This allows the hand-set to have only one oscillator which may jump between the RX and TX frequencies alternatingly. If, however, the distance between the RX and TX slots is too short, like in multi-slot mode, multiple oscillators must be used. This immediately has a power consumption penalty.

An attractive alternative to FDD is the time-division duplex (TDD) used in, for example, DECT. Here, RX and TX data is received and transmitted alternatingly at the same frequency. Then the slot distribution does not have an impact on the oscillator configuration. Furthermore, less filters are needed as the RX and TX frequencies are the same.

Finally, the page-scan frequency has a direct influence on the stand-by current consumption. It is, however, not sufficient to have long time between page scans. The hand-set must also be allowed to go into deep sleep between page scans. During these deep sleep periods the whole radio, except for one low-power timer, would be switched off. A crystal oscillator may consume one mA or more, which is too much for stand-by mode. Thus, the clock also has to be switched off.

### 4. Digital design techniques

The baseband (digital) circuit power dissipation is mainly due to three effects: node charging, leakage or bias currents, and crowbar (short-circuit) current. The design techniques one can use to reduce the current drain address each of the power-loss terms of Table 1. The well-known recipe is to reduce the supply voltage (or logic swing), node capacitance, node frequency and node transition times.

In a cellular phone, the baseband current consumption is dominated by node charging and in particular the driving of external buses. Internally, a typical bus-node capacitance may be 1–5 pF. An external (non-bus) signal may correspond to 5–10 pF and an external data bus anything from 30 pF to 70 pF. Often the designer’s options are limited by the available circuit libraries and by signal requirements from external chips, such as memories.

By splitting data buses into internal and external segments and inserting latches in-between, one can save much power in a fashion that is compatible with standard circuits. When no external signals are required, the internal and external buses are decoupled and the signal activity is confined to the internal bus. This corresponds to a reduction of the driven node capacitance by, typically, an order of magnitude. When an external bus is driven, the traditional load is seen. However, when the external bus is read, the bus value is written back by the latch circuit. Thus, the bus voltage will not change after it has been read but only when necessary. This read-and-write-back scheme reduces the bus activity substantially.

Another well-known and efficient technique for reducing the switching activity is to gate clocks. By gating a clock, only the relevant part of a circuit, or system, is clocked and the

<table>
<thead>
<tr>
<th>Cause</th>
<th>Power</th>
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<tbody>
<tr>
<td>node charging</td>
<td>( \propto fCV^2 ) dominant component</td>
</tr>
<tr>
<td>leakage and bias</td>
<td>( \propto IV ) static load, analog functions</td>
</tr>
<tr>
<td>crowbar current</td>
<td>( \propto fV^3t ) rise-time dependent, 5–30% of total power, floating nodes</td>
</tr>
</tbody>
</table>

**TABLE 1. Baseband-circuit power dissipation sources.**
The rest of the circuit remains idle without any dynamic power consumption. A possible alternative to gated clocks might be to use asynchronous circuits. An asynchronous circuit, however, typically has a substantial overhead compared to a synchronous circuit. Since data, and thus circuit activity, is bursty in known ways in cellular phone applications, it is possible to control clock gating efficiently and this technique offers lower current consumption.

Careful floor planning, partitioning of global functions, and splitting of global signals are also necessary steps in the design of baseband circuits.

5. Analog and RF design

RF, and other analog, power consumption is primarily set by the required dynamic range and the signal frequency.

The lower limit of the dynamic range is set by thermal noise in the radio low-noise amplifier (LNA). Noise matching is very important as it sets the sensitivity of the receiver and thus the reception quality under weak signal conditions. Amplifier noise is expressed by the noise factor (or noise figure if expressed in dB) which indicates by what factor the noise level is increased by the amplifier compared to the source (antenna) thermal noise [2].

With the FET, the designer can compromise between dynamic range and current. If the device is operated at a high gate bias, $V_{GS} - V_{th}$, the FET will be linear and have a high transit frequency, $f_T$, but also high current consumption due to the low $g_m/I_Q$ ratio. A low gate bias reduces the quiescent current and $f_T$ for a given transconductance (noise matching). When the FET approaches the subthreshold region it will have roughly the same characteristics as the bipolar transistor. In fact, the FET will probably have to run close to subthreshold, or in moderate inversion, to be able to compete with the bipolar device for integrated LNA applications.

In case of the bipolar transistor, the designer has fewer design options to meet dynamic range and current consumption specifications. The base spreading resistance acts like a resistor in series with the signal, so a low-$r_b$ device will have to be chosen, or several devices must be connected in

<table>
<thead>
<tr>
<th>FET</th>
<th>BJT</th>
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<tbody>
<tr>
<td>$F = 1 + \frac{2}{3g_m R_S} (1 + (\omega c_i R_S)^2)$</td>
<td>$\left(1 + \frac{r_b}{R_S}\right) \left(1 + \frac{g_m}{2g_m(r_b + R_S)} \cdot \left(1 + \frac{g_m^2 (r_b + R_S)^2 + g_m (r_b + R_S)}{\beta_0} + (\omega (r_b + R_S) c_i)^2\right)\right)$</td>
</tr>
<tr>
<td>$g_{m_{opt}} \left(\frac{1}{R_s f} = \frac{\mu (V_{GS} - V_{th})}{R_s \omega L^2}\right)$</td>
<td>$\frac{V_T}{r_b + R_S} \leftrightarrow \omega \sqrt{\frac{V_T}{\beta_0}} (c_i + c_\mu)$</td>
</tr>
<tr>
<td>$\frac{g_m}{I_Q} = \frac{2}{V_{GS} - V_{th}} \frac{1}{V_T}$</td>
<td></td>
</tr>
</tbody>
</table>

Table 2. Simplified FET and bipolar characteristics.
parallel. In practice, it is not possible to run the device at the $f_T$ peak, so a much lower collector current must be chosen. Typically, devices with an $f_{max}$ much larger than $f_T$ are suitable low-noise devices, and the best operating point is where the $f_T$ is just high enough for achieving a reasonable gain.

If the bipolar LNA is not linear enough when noise-matched, its impedance level has to be decreased ($g_m$ increased). Since the nonlinearity is normalized to $V_T$, a lower input voltage means less modulation of the device. Current consumption will, however, increase as much as $g_m$.

Local feedback may be employed to improve linearity but the loop gain is often too low, or noise will increase prohibitively.

An attractive solution to the LNA optimization problem is to use dynamic bias or to dynamically reconfigure the circuit according to the signal conditions. Weak signals would call for large devices (large $g_m$ and also low $r_b$ for BJTs) with a higher current consumption. When signal conditions are better, bias current can be reduced, or devices disconnected. So far, this approach has not been widely employed because of problems with input matching and noise added by the dynamic control circuits.

Although the RF discussion has been concentrated on LNA issues, the same questions are valid for mixers, oscillators, and other analog circuits. At the LNA input the noise and impedance level is determined by the antenna and matching network. On chip, however, the designer has more degrees of freedom. The upper signal level is often given by the supply voltage. From this upper limit, the noise floor can be computed. If this noise floor is given in volts it is possible to compute the required node capacitance from the relation

$$v_n^2 = kT/C$$  [2]. This relationship yields the minimum capacitance needed to lower the thermal noise below a given threshold and, hence, also the minimum current consumption. Of course, depending on circuit structure, a certain design margin and topology factor has to be applied.

A consequence of the $kT/C$ limit is that the current consumption will increase for analog circuits when the supply voltage is decreased. This is so because the noise floor has to track the supply rail and a lower noise floor calls for a higher capacitance and, thus, a higher current consumption. This is in direct contrast with digital circuits where lower supply voltages are desirable, especially when FET-devices are subject to velocity saturation (there is no speed penalty in lowering the supply voltage as long as the device is velocity saturation). For this reason it seems likely that cellular phones will have to incorporate mechanisms for providing different voltages; say 2.5 V to the analog/RF parts and 1.5 V to the baseband parts.

References


<table>
<thead>
<tr>
<th>FET</th>
<th>BJT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_Q$ ($F = 1.2$)</td>
<td>$\frac{5(V_{GS} - V_{th})}{3R_S} = 30$ mA</td>
</tr>
<tr>
<td>$\frac{V_{T}g_0}{r_b + R_S} = 4$ mA</td>
<td></td>
</tr>
<tr>
<td>$IP_3$</td>
<td>$\frac{V_{GS} - V_{th}}{\eta} = 23$ dBm</td>
</tr>
<tr>
<td>$\sqrt{8}V_T = -10$ dBm</td>
<td></td>
</tr>
<tr>
<td>$f_T$</td>
<td>$\frac{\mu_0(V_{GS} - V_{th})}{1.7 \cdot 2\pi L^2} = 12$ GHz</td>
</tr>
<tr>
<td>$\frac{g_m}{2\pi(C_{mu} + C_{pi})} = 12$ GHz</td>
<td></td>
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</tbody>
</table>

TABLE 3. Typical BiCMOS FET and bipolar data.