An Efficient Statistical Analysis Methodology and Its Application to High-Density DRAMs

Sang-Hoon Lee, Chang-Hoon Choi, Jeong-Taek Kong, Won-Seong Lee, and Jei-Hwan Yoo

Semiconductor R & D Center, Samsung Electronics Co., Ltd.
San #24 Nongseo-Ri, Kiheung-Eup, Yongin-Si, Kyungki-Do, Korea
e-mail : tcad@semigw.semi.samsung.co.kr

Abstract

In this work, a new approach for the statistical worst case of full-chip circuit performance and parametric yield prediction, using both the Modified-Principal Component Analysis (MPCA) and the Gradient Method (GM), is proposed and verified. This method enables designers not only to predict the standard deviations of circuit performances but also track the circuit performances associated with the process shift using wafer test structure measurements. This new method is validated experimentally during the development and production of high density DRAMs.

1 Introduction

As the device feature size of VLSI shrinks with new technologies, the relative variability of the process makes the circuit performances more sensitive to the fluctuations in process steps. Accordingly, the statistical circuit design methodology becomes extremely crucial for designers to meet the circuit performances to the tight specification across the entire range of process fluctuations. However, the applications of true statistical techniques are limited to the research stage or a few special purpose circuits [1] and most designers still rely on the conventional method. The previous works for statistical design can be categorized as follows:

· the statistical modeling of SPICE parameters
· the simulation techniques for yield prediction

An important task in developing a statistical SPICE model is the identification of the critical model parameters and the translations of the physical process variations into the SPICE model. For examples, Bolt et al. [2] and Cox et al. [3] attempted to describe the total MOSFET variances in terms of the inter-die variances of four physically meaningful parameters: channel length, channel width, flat-band voltage, and gate oxide thickness. Since these parameters are determined by different steps in the manufacturing process, they can be assumed to be statistically independent. The rest model parameters can be expressed as functions of these four parameters to account for model parameter correlations. However, each SPICE model parameter for empirical models such as BSIM or HSPICE level 28 cannot be represented as a function of these physically meaningful parameters. Therefore, an incomplete work on treating statistical SPICE model parameters could lead to erroneous conclusions in statistical analysis and optimization. Furthermore, it cannot trace the parametrized SPICE model associated with the process shift which frequently occurs in the development of products.

Statistical simulation techniques are essential for estimating yields, designing manufacturable and robust systems, deriving worst-case models, and testing. The most widely used technique for performing the statistical characterization is the Monte Carlo analysis [4]. Unfortunately, the accuracy of the result produced using the Monte Carlo analysis is only proportional to the square root of the number of design variables and statistical parameters. Moreover, the number of Monte Carlo simulations required to produce a relatively accurate result increases exponentially with the number of statistical variables. Therefore, the Monte Carlo analysis is too expensive to apply to the real VLSI designs at the full-chip level.

One promising approach to deal with these shortcomings is proposed in this paper. In this design methodology, two statistical methods, the Modified-Principal Component Analysis (MPCA) and the Gradient Method (GM), are used and verified throughout various experiments. First, we have used a technique incorporating the Principal Component Analysis [5], which takes the distributions of SPICE parameters and electrical test measurements (E-tests) as inputs. Thus, each SPICE model parameter can be expressed as a function of independent E-tests. Then, the Gradient Method [2, 6] is used to predict the standard deviations of circuit performance with a few independent E-tests.

We present our statistical characterization system for prediction of yield distribution in Section 2. In Section 3, the Principal Component Analysis and the Gradient Method for our methodology are introduced at the point of the mathematical formula. In Section 4, an experimental qualification of the method is discussed based on the development and VLSI products such as the full density test vehicle of 256 Mbit DRAMs. Finally, we summarize this work in Section 5.

0-89791-993-9/97 $10.00 © 1997 IEEE

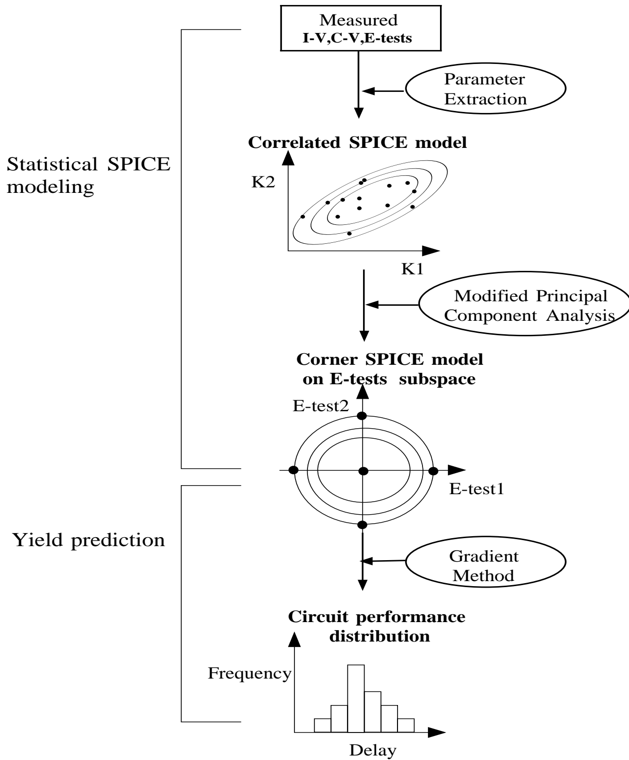

Figure 1: A global view of the statistical characterization system

2 The Statistical Characterization System for Worst Case Corners

A global view of the product design and characterization process is shown in Fig. 1. The proposed procedure constists of two parts: statistical SPICE modeling with parameter extraction and yield prediction.

First, APEX [7], which uses a nonlinear optimization method [8], automatically extracts SPICE model parameters from the database for I-V, C-V and E-tests together with the device geometries and layout design rules. After parameter extraction with mapping the process variations to SPICE model parameters, pdPCA [9, 10], a commercial tool exploiting correlations between parameters, interprets the covariance of correlated SPICE model parameters. Using pdPCA, we can derive a few independent E-tests which account for the total variance in SPICE model parameters. The SPICE model parameters can be expressed as functions of the critical independent E-tests.

After this, we can treat circuit performances as functions of reduced orthogonal spaces of E-tests, instead of fully correlated spaces of SPICE model parameters and deduce the relationship between the E-tests and circuit performances, geometrically and effectively. This result can be directly applied to the Gradient Method (GM), which lead to a more efficient prediction of circuit performances.

3 The Statistical Modeling Approach

3.1 Modified Principal Component Analysis

The Principal Component Analysis is a technique of transforming the correlated variables into uncorrelated variables, called principal components. Using this, each variable is a linear or nonlinear combination of the principal components. Thus, if $p_1, ...p_n$ are the principal components for n normalized response variables $x_1, x_2...x_n$, then the following formula for principal components (p_j) can be determined using the principal components analysis:

$$x_i = u_{i1}p_1 + u_{i2}p_2 + ... + u_{ij}p_j + ...u_{in}p_n \qquad (1)$$
$$i, j = 1, 2, ...n$$

where
x_i is the ith SPICE model parameter,
p_j is the jth principal component and
u_{ij} is the loading value of x_i on p_j
(i.e., the correlation between x_i and p_j).
The coefficient u_{ij} is chosen to satisfy 2 requirements:

$$Var(p_i) > Var(p_j) \ where \ i > j \ \ and \qquad (2)$$

$$p_i \ \cdot \ p_j \ = \ 0 \ (i \neq j). \qquad (3)$$

Eq. (2) implies that the principal components are arranged in the order of decreasing variances and the most informative principal component is the first, and the least informative is the last. On the other hand, the variance of p_1 is as large as possible. Eq. (3) is important to deal with statistical simulation techniques because we want to express the circuit performance in terms of statistically uncorrelated, independent parameters [2, 3]. Therefore, based on the principal components, the original covariance of correlated SPICE model parameters can be explained by a few independent principal components (or pseudo parameters). However, these pseudo parameters represented in Eq. (1) from the traditional PCA are of no use because we cannot understand a physical meaning of them. Knowing the physical interpretation would enable us to track how changes in the process impacts circuit performance. It should be noticed that the principal components result statistically from the existence of a set of low level, independently varying physical quantities, called the process disturbances [11], that affect each process step in terms of the statistical variations of an IC process. However, since process disturbances are nonmeasurable quantities in general, a matching algorithm [12, 13], which looks for similarities between the principal components and E-tests, was incorporated in this work in order to replace the principal components with E-tests having the largest correlation value.

3.2 The Gradient Method

Despite of potential benefits of statistical design, it is difficult to apply it to statistical prediction of full-chip circuit performance because all statistical design

tools and algorithms are too expensive in computational and engineering efforts. Therefore, a worst case design method to predict the standard deviations of circuit performances is more effective in terms of simulation time. The Gradient Method [2, 6] can be used to predict the standard deviation of the circuit performance. It amounts to the following problems:

$$z = f(x_1, x_2 ...) \quad (4)$$

where z is the simulated circuit performance (response) and x_i is an input parameter (design variable or SPICE model parameter). The standard deviation of circuit performance z can be predicted as:

$$\sigma_z = \sqrt{(\frac{\partial z}{\partial x_1})^2 {\sigma_{x1}}^2 + (\frac{\partial z}{\partial x_2})^2 {\sigma_{x2}}^2 + \cdots} \quad . \quad (5)$$

The expression of Eq. (5) is valid, if the input parameters are independent each other and the circuit performance z is a linear function in 3 σ window of component-space x_i (this assumption will be verified throughout experiments). In this simple equation, the standard deviation σ_{x_i} of x_i is measured and the gradient $\frac{\partial P}{\partial x_i}$ is calculated using circuit simulation. Therefore, the statistical distribution of the circuit performance can be estimated using GM with the minimum number of statistically uncorrelated independent factors that represent the variability in SPICE model parameters using MPCA.

4 Experimental Results

To demonstrate the use of statistical analysis on equivalent full-chip circuits of DRAMs, the circuit performances t_{RAC}, which is defined as the time-interval between RAS (Row Address Strobe) and DOUT (Data Out), was analyzed in the page mode operation. The primary interest for this example is the variation in the time delay t_{RAC} as a function of the statistical device parameters.

4.1 Worst Case Design

The measurements for this work consist of I-V/C-V curve collections and E-tests with temperature of 357 K. Table 1 lists the number of the devices and the SPICE model parameters for the parameter extraction and the statistical SPICE modeling. All sixteen devices (i.e, eight nMOSFETs and pMOSFETs) were included in this experiment. To determine the repeatability of the parameter extractor, many sets of 31 and 38 model parameters for nMOSFETs and pMOSFETs were extracted for the same device size. The simulation results using extracted SPICE model parameters agree well with the actual curves for both nMOSFETs and pMOSFETs, as shown in Fig. 2. The average RMS (Root of Mean Square) errors for sixteen devices is less than 5%. The total 69×69 correlation matrix for SPICE model parameters was obtained in order to preserve dependencies between nNMOSFET and pMOSFET. As described in the previous section,

Table 1: The number of transistors and HSPICE level 28 parameters used for parameter extraction

	NMOS	PMOS
The number of MOSFETs	8	8
The number of SPICE parameters	31	38

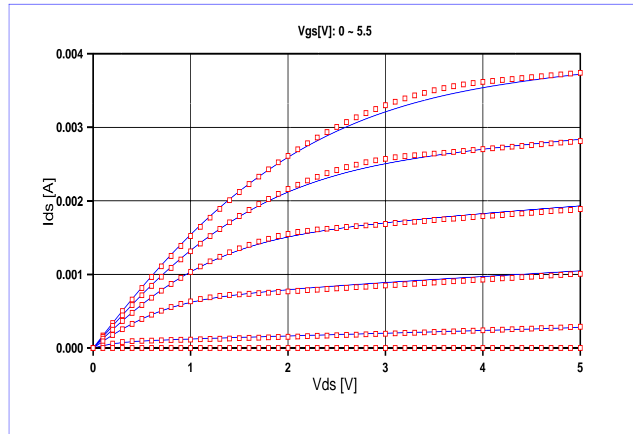

Figure 2: I-V characteristics of measured (line) and calculated (symbol) data of L = 0.35 μm nMOSFET

we apply pdPCA to determine the minimum number of statistically uncorrelated independent factors that represent the variability in SPICE model parameters.

As shown in Fig. 3 [10], total 12 principal components account for 100% of total variances in SPICE model parameters and each SPICE model parameter can be represented as a function of those, as in Eq. (1). Using the matching algorithm [13], the first 4-components can be replaced with Gmmax of L = 0.40 μm pMOSFET (G_{mmax}), the junction capacitance of n^+p type (C_j), the sheet resistance of plate poly (R_{spp}), and the threshold voltage of L = 25 μm pMOSFET (V_{th}), as shown in Fig. 4. The first factor accounts for 34% of the variance of the key I-V points and device physicals (E-tests and SPICE model parameters). The first factor mainly accounts for the variance of gate oxide thickness (TOXM), linear Vds threshold coefficient (ETA0), weak inversion factor (WFAC), back bias correction (X2M), and mobility reduction related sensitivity parameters (LU0 and LU1). Similarly, factors 2, 3, and 4 account for 15%, 12%, and 11%, respectively.

In Eq. (5), the GM is modeled assuming that the circuit performance is a linear function of principal components. This assumption has been verified using measurements for t_{RAC} versus the first component variation, as shown in Fig. 5. In this plot, we have observed that t_{RAC} can be approximated as a linear function of the first component (Gmmax). In [14], the algorithms are investigated in the case that the data points look like they could be better fit with a

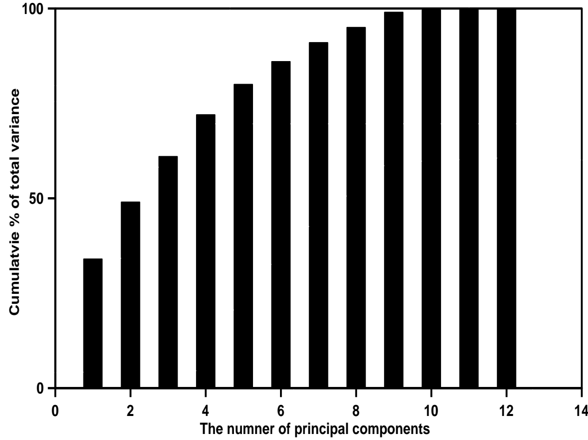

Figure 3: Cumulative percentage of total variances in SPICE model versus the selected number of principal components

	FACTOR1	FACTOR2	FACTOR3	FACTOR4	
Tracking E-tests	Gmmax	Cj	Rspp	Vth	SUM[%]
Ave.	34.0	15.0	12.0	11.0	72.0
toxm	90.8	1.3	2.2	0.0	94.3
eta0	78.6	4.8	1.8	0.0	85.2
k1	43.5	0.1	9.6	0.2	53.4
k2	1.6	3.3	26.2	10.1	41.1
muz	12.6	15.1	4.5	45.4	77.6
phi0	14.3	30.8	0.7	13.7	59.4
u00	1.9	15.1	12.3	7.6	36.9
u1	0.0	5.3	20.4	25.9	51.7
vfb0	45.7	33.7	0.1	0.3	79.9
wfac	76.8	1.1	1.4	7.4	86.6
x2m	82.6	0.6	0.1	1.2	84.5
leta	19.5	1.9	40.6	1.8	63.9
lk1	28.8	11.9	15.7	26.5	82.9
lk2	7.2	2.6	22.9	44.5	77.2
lmuz	5.9	1.2	25.0	51.7	83.8
lu0	72.0	1.1	12.6	1.0	86.7
lu1	80.4	0.7	4.5	0.7	86.3
lvfb	17.0	30.4	0.4	0.1	47.8
wk1	13.9	20.1	15.1	13.0	62.2
wk2	5.3	10.2	7.5	39.1	62.1
wmuz	51.1	4.9	20.8	7.3	84.1
wu0	26.3	8.1	0.2	9.1	43.7
wu1	0.2	25.7	23.8	6.2	55.9
wvfb	37.6	12.5	14.4	17.6	82.1
cj	2.3	88.0	5.9	0.1	96.3
cjsw	87.2	1.9	5.7	4.2	99.0
pb	4.3	22.2	31.5	8.6	66.6
mj	12.8	44.1	15.6	6.0	78.5
php	86.1	3.0	2.8	4.4	96.3
njsw	88.5	1.7	3.5	4.5	98.0
CGSO	35.5	0.2	6.1	12.1	54.0

Figure 4: Percentages of the HSPICE level 28 parameter variances which can be monitored by E-tests for nMOSFETs

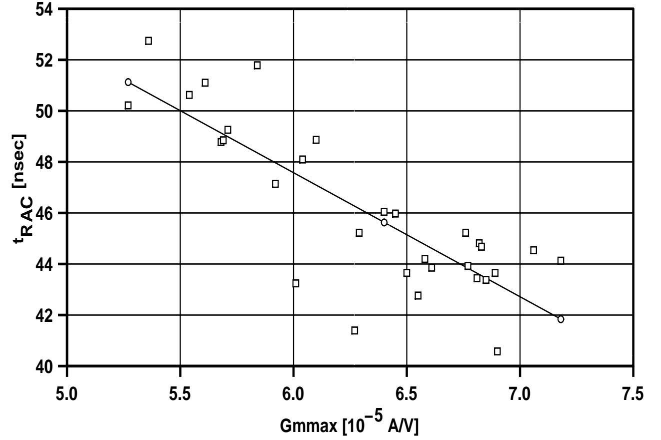

Figure 5: Experimental (box symbol) read access time, t_{RAC}, versus Gmmax of L = 0.40 μm pMOSFET (The solid line is a linear interpolation of data.)

piecewise-linear function.

As an example of the proposed approach, we compared the variations of t_{RAC} of 256 Mbit DRAMs with the predicted performances. The typical set of SPICE model parameters for the nominal design was determined by setting a mean value of G_{mmax}, C_j, R_{spp}, and V_{th} from measured data in Eq. (1). Then, best/worst values of t_{RAC} for statistical design can be obtained using GM. It is shown that the predicted performance variations agree well with the measured variations, as shown in Fig. 6.

Table 2 shows the comparison of the old method [2, 3, 15] and the new method. The old method uses the physically measurable model parameters and the key parameters in order to predict the actual circuit response to the extreme conditions of a manufacturing process. These physically measurable model parameters are called skew parameters [15] or principal factors [3]. The skew parameters are generally chosen to be independent of each other so that the combinations of skew parameters can be used to represent the worst case. The typical skew parameters for a CMOS technology include:

- XL - poly silicon variations
- XW - active width variations
- TOX - gate oxide thickness variations
- RSH - active layer resistivity variations
- DELVTO - threshold voltage variations

The worst case is simulated by taking all variables to their 2-σ or 3-σ worst case value (3-σ in this work). From Table 2, the new method models the real distribution of t_{RAC} more accurately than the old method.

4.2 The Estimation of the Process Shift Effects

The proposed method is also applied to 64 Mbit DRAMs. In this case, we have found that the first 4 components account for 75% of the total variance in

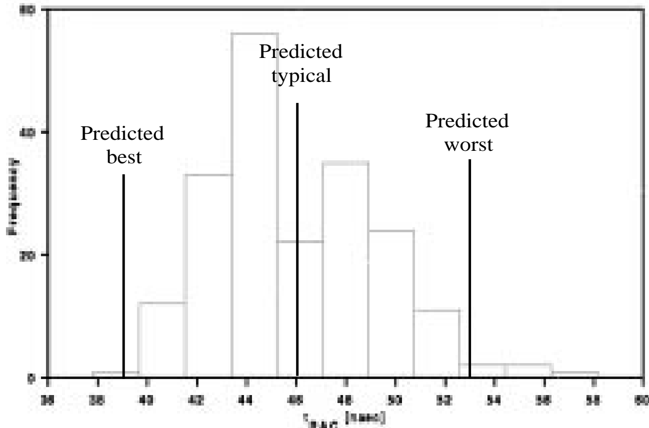

Figure 6: Experimental (bars) and simulated (lines) read access time, t_{RAC}, from 256 Mbit DRAM

Table 2: The comparison of thw new method and the old method

t_{RAC} [ns]	measured	new method	old method
best	39	39	41
typical	46	46	46
worst	57	53	52

the process variations and these components can be replaced with Tox, Vth and so on using the matching algorithm. From this result, we can resolve the problems related to the process shift. Actually, under development of the CMOS DRAM, gate oxide thickness (Tox), the channel implant for nMOSFETs, and heat annealing conditions were changed in order to obtain the margin of electrical characteristics on the dynamic condition of some critical circuits. The changed process conditions are shown in Table 3. From a parameterized SPICE model associated with some E-tests, a unified approach to SPICE model parameter monitoring can be maintained as the process shifts. Thus, the model parameter set corresponding to the process shift can be determined. In order to verify the shift model parameters, the threshold voltage and saturation current of L = 0.40 μm nMOSFET and L = 0.45 μm pMOSFET are shown in Table 4. The predicted values of V_{th} and I_{dsat} agree well with the measured values. In Table 5, the experiments and simulation results are compared. We can see that the calculated value of t_{RAC} agrees well with experimental data while the traditional method does not provide this result.

Yield estimation has been performed on the same product with an inexpensive Monte Carlo analysis [1, 16, 17]. As mentioned previously, since only a few statistical variables are responsible for the most of the process-induced variations on circuit performances, the parametric yield can be estimated efficiently using the RSM [18] model and the Monte Carlo analysis. Circuit simulations are performed by sampling from the normal distributions of the principal

Table 3: The conditions of process shifts

Process	Changed rate [%]
Channel dose	-10
Field-stop dose	12.5
Gate oxide thickness	11
Heat cycle time	100

Table 4: Calculated and measured Vth [V] and $Idsat$ [mA] of NMOS and PMOS

	NMOS		PMOS	
	Vth	$Idsat$	Vth	$Idsat$
Measured	0.58	2.27	0.80	1.07
Calculated	0.60	2.28	0.80	1.15

Table 5: The comparison of measured and calculated typical t_{RAC}[ns]

Measured	Calculated	Error rate[%]
43	42.4	1.5

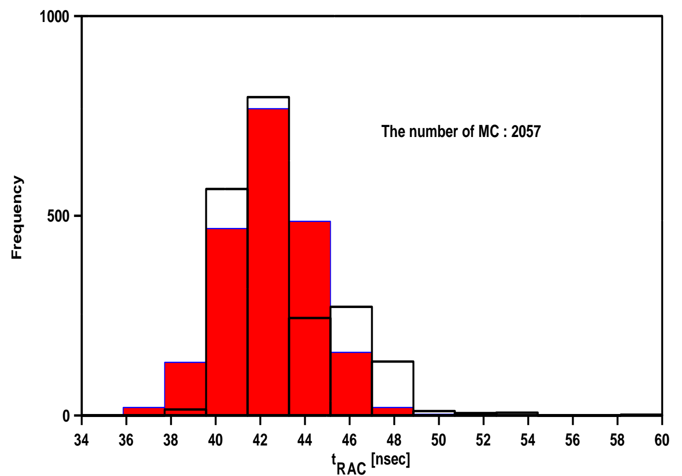

Figure 7: The comparison of measured (white bars) and predicted (black bars) distribution of t_{RAC}

components which are the results of PCA. Because it is sufficient to fit the linear model to the relationship between circuit performances and E-tests, we apply an Orthogonal Array (OA) design [19] which does not consider interactions of two variables. In the examples, the corresponding yield was estimated to be approximately 90% with 2057 Monte Carlo runs, as shown in Fig. 7. The measurement estimation gives us the yield of 80%.

5 Conclusions

An efficient methodology for yield prediction of full-chip circuit performance has been described in this paper. These algorithms are based on the Modified-Principal Component Analysis the and the Gradient Method. There are several distinct features in this work: 1) the Gradient Method allows a great simplification in obtaining the statistical worst case of full-chip circuit performance, 2) this methodology enables designers to track the circuit performance according to the process shift using measured E-tests, and 3) the parametric yield can be estimated effectively with an inexpensive Monte Carlo analysis without any need for the usual multitude of circuit simulations. Throughout the application to the full-chip circuits of high density DRAMs, it is proved that the new method provides designers with the accurate distributions of circuit performance and yield prediction.

Acknowledgments

The authors would like to thank Soon-Cheol Hong, Won-Woo Lee, and Jin-Kyu Park for valuable discussions and measurements. We would also like to thank Dr. Kyung-Ho Kim and Dr. Soo-In Cho who originally initiated and inspired this project.

References

[1] S. G. Duvall, "A practical methodology for the statistical design of complex logic products for performance," *IEEE Trans. VLSI Systems*, vol. 3, pp. 112–123, Jan. 1995.

[2] M. Bolt, M. Rocchi, and J. Engel, "Realistic statistical worst-case simulation of VLSI circuits," *IEEE Trans. Semiconductor Manufacturing*, vol. 4, pp. 193–198, Aug. 1991.

[3] P. Cox, P. Yang, S. S. Mahant-Shetti, and P. Chatterjee, "Statistical modeling for efficient parametric yield estimation of MOS VLSI circuits," *IEEE Trans. Electron Devices*, vol. ED-32, pp. 471–478, Feb. 1985.

[4] S. W. Director and G. D. Hachtel, "The simplicial approximation approach to design centering," *IEEE Trans. Circuits Syst.*, vol. CAS-24, pp. 363–372, July 1977.

[5] D. F. Morrison, *Multivariate Statistical Methods*, New York:McGraw-Hill, 1976.

[6] S. H. Lee, K. H. Kim, J. K. Park, C. H. Choi, J. T. Kong, W. W. Lee, W. S. Lee, J. H. Yoo, and S. I. Cho, "A realistic methodology for the worst case analysis of VLSI circuit performances," in *Int. Conf. on Simulation of Semiconductor Process and Devices*, pp. 155–156, 1996.

[7] C. H. Choi, J. K. Park, Y. G. Kim, K. H. Kim, and S. H. Lee, "New model parameter extraction environment for the submicron circuit models," *IEEE International Symposium on Circuit and Systems*, pp. 1535–1538, 1993.

[8] K. Doganis and D. L. Scharfetter, "General optimization and extraction of IC device model parameters," *IEEE Trans. Electron Devices*, ED-30, pp. 1219–1228, 1983.

[9] *pdPCA User's Manual*, PDF Solutions, 1996.

[10] D. A. Hanson and R. J.G. Goossens, "Analysis of Mixed-Signal Manufacturability with statistical TCAD," in *Int. Symp. on Semiconductor Manufacturing*, pp. 271–276, 1995.

[11] C. J. B. Spanos and S. W. Director, "Parameter extraction for statistical IC process characterization," *IEEE Trans. Computer-Aided Design*, vol. CAD-5, pp. 66–78, Jan. 1986.

[12] C. R. Shyamsundar, P. K. Mozumder, and A. J. Strojwas, "Statistical control of VLSI fabrication processes: a software system," *IEEE Trans. Semiconductor Manufacturing*, vol. 1, pp. 72–82, May 1988.

[13] J. Kibarian, "Statistical diagnosis of IC process faults," Ph. D. dissertation, CMUCAD 90-52, December 1990.

[14] Mien Li and Linda Milor, "Computing Parametric Yield Adaptively Using Local Linear Models," in *Proc. of the 33rd Design Automation Conference*, pp. 831–836, 1996.

[15] *HSPICE User's Manual*, Meta Software, 1996.

[16] T. K. Yu, S. M. Kang, I. N. Hajj, and T. N. Trick, "iEDISON: An interactive statistical design tool for MOS VLSI circuits," in *Proc. IEEE Int. Conf. Computer-Aided Design*, pp. 20–23, Nov. 1988.

[17] L. Milnor and A. Sangiovanni-Vincentelli, "Computing parametric yield accurately and efficiently," in *Proc. IEEE Int. Conf. Computer-Aided Design*, pp. 116–119, 1990.

[18] R. H. Myers and D. C. Montgomery, *Response Surface Methodology: Process and Product Optimization Using Designed Experiments*, John Wiley and Sons, New York, 1995.

[19] A. Dey, *Orthogonal Fractional Factorial*, New York: Halsted Press, 1985.