A New CMOS Tunable Transconductor Dedicated to VHF Continuous-Time Filters

Ali ASSI, Mohamad SAWAN and Rabin RAUT*
Ecole Polytechnique de Montréal
P.O. Box 6079, Station "Centre-ville", Montreal, PQ, Canada, H3C 3A7
*Concordia University, Montreal, Canada

Abstract

A new CMOS transconductance (Gm) circuit with voltage-tunability and very wide bandwidth is proposed and analysed. The transconductance circuit is then used to realize a tunable VHF 2nd-order bandpass filter cell. The center frequency (f0) of the designed filter can be tuned by varying the transconductance value (gm) of the tunable GM circuit. Simulation results indicate the excellent performances of both the transconductance circuit and the filter over a wideband range. The transconductance value can be tuned from 40μS to 950 μS (490 μS) and the filter center frequency (f0) in the range 30 MHz (4 MHz)-110 MHz (49 MHz) for ±2.5V (±1.5V) supply voltages.

1. Introduction

Transconductors are usefull building blocks for a variety of continuous-time signal-processing circuits. The continuous-time filters are one of the potential circuits build with trandconductance elements and capacitances. In the design of high-frequency circuits involving transconductors, many important characteristics (bandwidth, power consumption, tunability, etc...) are to be considered. Several transconductor designs have been reported for high-frequency continuous-time signal-processing applications [1]-[2]. In [1] the bandwidth of the reported transconductor is limited by the internal nodes in the circuit, which results in parasitic poles or zeros and necessitates special techniques to compensate for these effects in the high-frequency range. The transconductor presented in [2] made use of the standard square-law model for MOS devices in their saturation region to achieve a large bandwidth circuit without internal nodes, however, the transfert function reported suffers from its dependency on the temperature dependent threshold voltages of the devices, also the tunability of the transconductor is achieved via the supply voltage which is not suitable for applications where the supply voltage should be fixed.

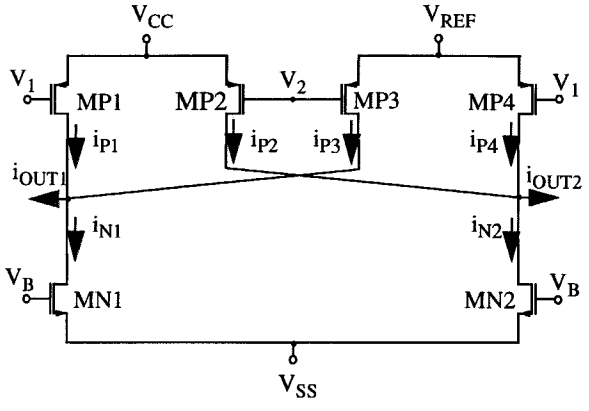

Fig. 1. The transconductance circuit.

In this paper, our interest is concentrated on the design of a transconductor with improved bandwidth and tunability. In fact, a new CMOS transconductance circuit for high frequency applications is proposed. As in [2], the circuit

presented here makes use of the square-law principle and has no internal nodes resulting in a very wide band operation [3]. The dependency of its transfert function on the threshold voltages is eleminated. The tunability is also improved and made possible without varying the main supply voltages (V_{CC} and V_{SS}). The remaining of the paper is organized as follows. Analysis of the proposed transconductance circuit is presented in section 2. Application to a bandpass biquad structure is presented as an example in section 3. Simulation results and conclusions are given in sections 4 and 5 respectively.

2. Transconductor analysis

Fig.1 shows the proposed transconductance circuit using six CMOS transistors interconnected in a fully differential structure. It is clear that the circuit has no internal nodes which is a desirable characteristic for high-frequency operation as mentionned in the previous section. The tunability of the transconductor is realized by varying V_{REF}, a desirable characteristic which will be demonstrated in the following analysis.

2.1. Large signal analysis

Assuming matching between the geometrically identical p-MOS devices MP1-MP4 and between the n-MOS devices MN1-MN2 and using the standard square-law model for MOS devices in their saturation region, the currents i_{OUT1} and i_{OUT2}, are easily derived as

$$i_{OUT1} = i_{P1} + i_{P3} - i_{N1} \quad (1a)$$

$$i_{OUT2} = i_{P2} + i_{P4} - i_{N2} \quad (1b)$$

where

$$i_{P1} = \frac{\beta_P}{2}\left(V_{CC} - V_1 - V_{TP}\right)^2 \quad (2a)$$

$$i_{P2} = \frac{\beta_P}{2}\left(V_{CC} - V_2 - V_{TP}\right)^2 \quad (2b)$$

$$i_{P3} = \frac{\beta_P}{2}\left(V_{REF} - V_2 - V_{TP}\right)^2 \quad (2c)$$

$$i_{P4} = \frac{\beta_P}{2}\left(V_{REF} - V_1 - V_{TP}\right)^2 \quad (2d)$$

$$i_{N1} = i_{N2} = \frac{\beta_N}{2}\left(V_B - V_{SS} - V_{TN}\right)^2 \quad (2e)$$

and

$$\beta_{N,P} = \left[\mu C_{ox}\left(\frac{W}{L}\right)\right]_{N,P} \quad (3)$$

is the transconductance parameter. μ , C_{ox}, V_{TN}, V_{TP}, W and L have their usual meaning. V_{CC} and $V_{SS} = -V_{CC}$ are the supply voltages , V_1 and V_2 are the input voltages and V_B is a biais voltage for the n-MOS transistors.

Thus with equations (1) and (2) , the differential output current $i_{OUT} = i_{OUT1} - i_{OUT2}$ equals (assuming a differential input $V_1 = V_d/2$, $V_2 = -V_d/2$, around a common mode signal CM=0)

$$i_{OUT} = -V_d\left[\beta_P\left(V_{CC} - V_{REF}\right)\right] \quad (4)$$

Equation (4) reveals the function of the circuit of fig.1 as a linear voltage to current transducer, $i_{OUT} = -g_{mT}V_d$, where

$$g_{mT} = \beta_P\left(V_{CC} - V_{REF}\right) \quad (5)$$

is the total transconductance parameter that can be controlled easily by varying V_{REF}. The tunability of the circuit via the difference V_{CC}-V_{REF} assumes that V_{CC} and V_{REF} are to be different, this leads to an N-well process for MP1, MP2 and MP3, MP4 built on separate N-wells. Equation (5) shows that the transconductor transfer characteristic does not involve the V_T of the transistors. Thus to a first order approximation, the operation will be insensitive to the variations in V_T. This is a clear advantage relative to the transconductors reported in [1]. In addition, since the source nodes are connected to respective substrates, the operation will not be influenced by the body effect.

2.2. Small signal analysis

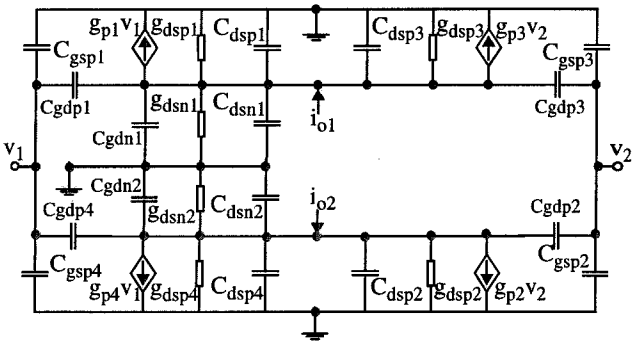

Fig.2. The ac equivalent model for the transconductance circuit.

The ac equivalent model of the proposed wideband transconductance circuit is shown in fig. 2. The short circuit (ac) output currents i_{o1} and i_{o2} are given by:

$$i_{o1} = v1\left(g_{p1} - sC_{gdp1}\right) + v2\left(g_{p3} - sC_{gdp3}\right) \quad (6a)$$

$$i_{o2} = v1\left(g_{p4} - sC_{gdp4}\right) + v2\left(g_{p2} - sC_{gdp2}\right) \quad (6b)$$

where

$$g_{pi} = \sqrt{2I_{Di}\mu_p C_{OX}\frac{Wi}{L}} \qquad (i = 1, 2, 3, 4)$$

are the transconductances, sC_{gpi} are the gate-drain parasitic capacitances of the corresponding devices.

Assuming a fully differential (ac) input signal (v_1=v/2, v_2=-v/2) around a common mode voltage vc = 0, the output current $i_{out} = i_{o1} - i_{o2}$ can be written as

$$i_{out} = \frac{v}{2}\left(g_{p1} + g_{p2} - g_{p3} - g_{p4} - sC_{gdp1} - sC_{gdp2} + sC_{gdp3} + sC_{gdp4}\right) \quad (7)$$

and an appropriate geometric arrangement of the devices to make

$$sC_{gdp3} + sC_{gdp4} = sC_{gdp1} + sC_{gdp2}$$

then, the output current i_{out} can be expressed as

$$i_{out} = \frac{v}{2}\left(g_{p1} + g_{p2} - g_{p3} - g_{p4}\right) \quad (8)$$

Thus the transconductor exhibits an (ac) transconductance which is constant to frequencies beyond 1 GHz as will be shown in the simulation results.

3. Filter Design

The basic building block of transconductance-C (G_m-C) filter is an integrator involving a transconductor and a capacitor. The integrator is usually characterized by its dc gain and its unity gain frequency $\omega_0 = G_m/C$. Deviations from the ideal -90° phase of the integrator are mainly due to finite dc gain and parasitic poles of the transconductance circuit [4]. For high-frequency filters which use the G_m-C approach, the frequency response is very sensitive to the phase shifts in the integrators. Therefore, to avoid deviations in the filter characteristics, a high-dc-gain integrator is required with parasitic poles located much higher than the filter cut-off frequency to keep the integrator phase at -90°.

Using the transconductance circuit of figure 1, the dc gain and the bandwidth of the derived integrator can be improved with a negative resistance load according to [5]. The resulting integrator block is shown in figure 3, where V_{CR} is a variable voltage used to tune the negative resistance load (NRL).

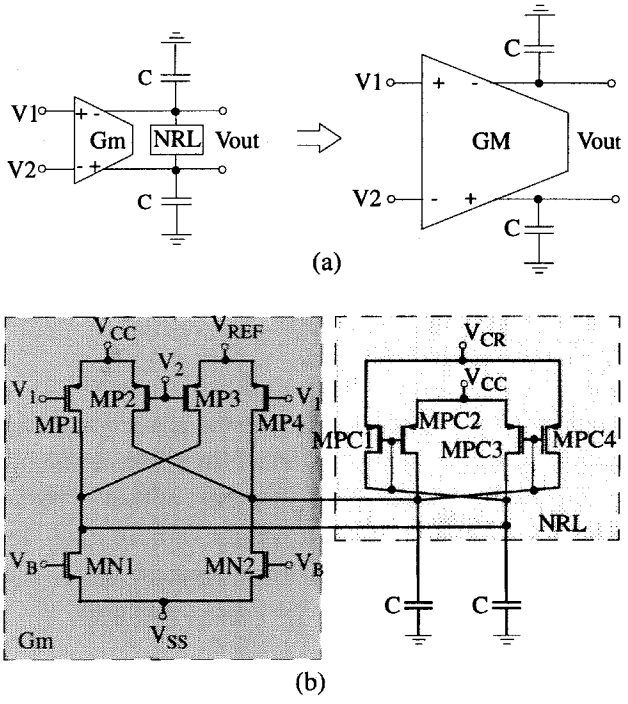

Fig.3. The transconductor-C integrator a) block diagram; b) complete schematic.

As an example of application of the proposed transconductor and integrator, a second-order (biquadratic cell) bandpass filter [6] has been designed. The schematic of the filter is shown in figure 4. The reader can verify that the circuit realizes the second-order bandpass function:

$$H_{BP}(s) = \frac{V_{out}}{V_{in}} = \frac{sCg_m}{C^2s^2 + sCg_m + g_m^2} = \frac{sM\frac{\omega_0}{Q_0}}{s^2 + s\frac{\omega_0}{Q_0} + \omega_0^2} \quad (9)$$

Equation (9) were writen in a form that shows explicitly the relevant filter parameters: the midband gain M of the bandpass, the pole frequency ω_0, and the pole quality factor Q_0. In particular,

$$\omega_0 = \frac{g_m}{C} \qquad (10)$$

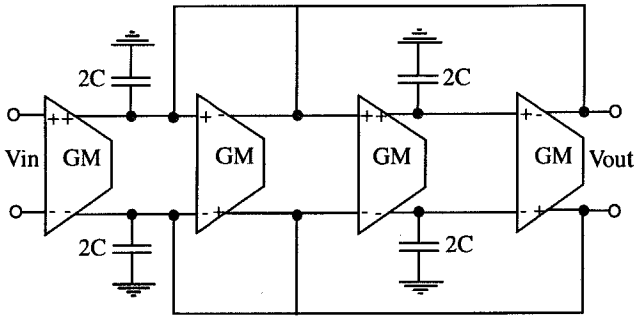

Fig.4. Filter structure.

4. Simulation results

HSPICE simulations for both the transconductance circuit as well as the bandpass filter have been carried out. In these simulations, SPICE parameters of the 0.8 micron BiCMOS technology (NORTEL) have been used. The transistors ratios are given in Table I and the supply voltages of $\pm 1.5V$, $\pm 2V$ and $\pm 2.5V$ have been used.

Table I. Dimensions (μm) of the transistors.

Transistors	W/L
MP1, MP2, MP3, MP4	45/1.4
MN1, MN2	20/2.4
MPC1, MPC2, MPC3, MPC4	10/3.4

Fig. 5 shows the tuning capability of of the transconductance circuit. The transconductance value can be tuned from 40 μS to 950 μS depending on the value of V_{CR} and the supply voltage used. Figure 5(b) shows clearly the wideband characteristic of the transconductance circuit, the value of gm is constant to frequencies beyond 1 GHz.

Varying V_{REF} from 0.9 V to 2.0 V (1.45 V) and consequently adjusting V_B and V_{CR}, the filter center frequency is tuned in the range 30 MHz (4 MHz)-110 MHz(49 MHz) for $\pm 2.5V$ ($\pm 1.5V$) supply voltages (Fig. 6). This shows the feasibility of the designed filter in the low-supply-voltage operation. For 1% THD, the equivalent maximum output signal of the filter with center frequency 110 MHz (49 MHz) is about 375 mV (185 mV) with a $\pm 2.5V$ ($\pm 1.5V$) supply voltages. Other simulation results are shown in Table II.

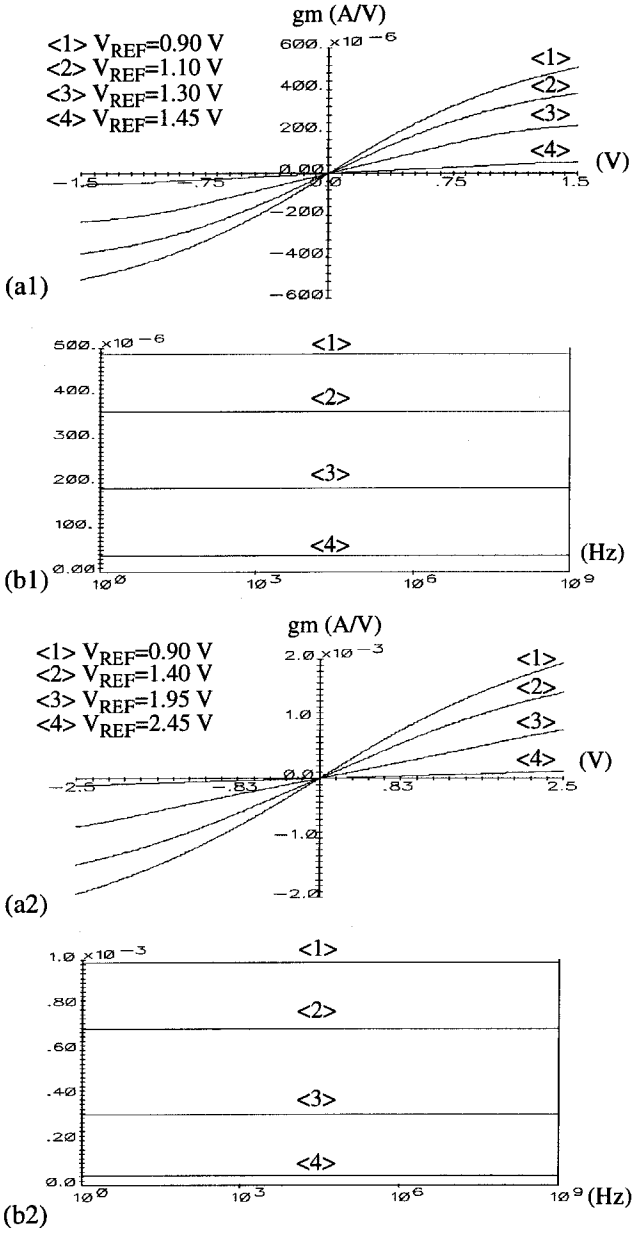

Fig.5. Tuning capability of the transconductance circuit; V_{REF} is taken as parameter

a) DC responses

a1) $V_{CC} = -V_{SS} = 1.5$ V; a2) $V_{CC} = -V_{SS} = 2.5$ V.

b) AC responses

b1) $V_{CC} = -V_{SS} = 1.5$ V; b2) $V_{CC} = -V_{SS} = 2.5$ V.

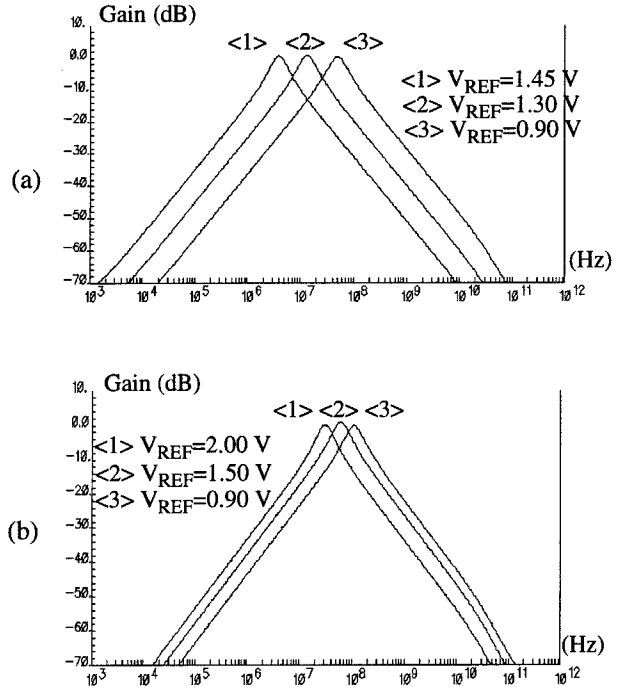

Fig.6. Simulated response of the bandpass biquad filter a) V_{CC} = -V_{SS} = 1.5 V; b) V_{CC} = -V_{SS} = 2.5 V.

The quality factor (Q) can be enhanced by cascading the biquads to form higher-order filters. Fig. 7 shows the frequency response of the fourth-order bandpass filter compared to that of a second-order bandpass biquad. The quality factor Q can be increased from 1.46(1.27) to 2.10(1.89) for $\pm 2.5V\,(\pm 1.5V)$ supply voltages.

5. Conclusion

A new tunable CMOS transconductor using six transistors and having a constant transconductance over a very wide bandwidth (~ 1 GHz) has been introduced. The proposed transconductor has been used and applied succefully to the design of a bandpass biquad filter suitable for VHF applications. The designed bandpass filter features a good tuning range of its center frequency (f0) 30 MHz (4 MHz) - 110 MHz (49 MHz) for $\pm 2.5V\,(\pm 1.5V)$ supply voltages. The control voltages (V_{REF}, V_{CR}, V_B), can be changed by on chip digital control or varied by means of some precision external resistor.

Table II. Simulated results of the bandpass filter.

	V_{CC}=-V_{SS}= 1.5 V	V_{CC}=-V_{SS}=2.5V
Capacitive Load	1 pF	1 pF
Control Voltages		
V_B	0.40 V	0.60 V
V_{CR}	1.016 V-1.039 V	1.000 V-1.136 V
V_{REF}	0.9 V-1.45 V	0.9 V-2.0 V
Center Frequency f0	4 - 49 MHz	30 - 110 MHz
Quality factor Q	1.3150 - 1.2915	1.7464 - 1.4620
Power consumption	5 mW	54 mW

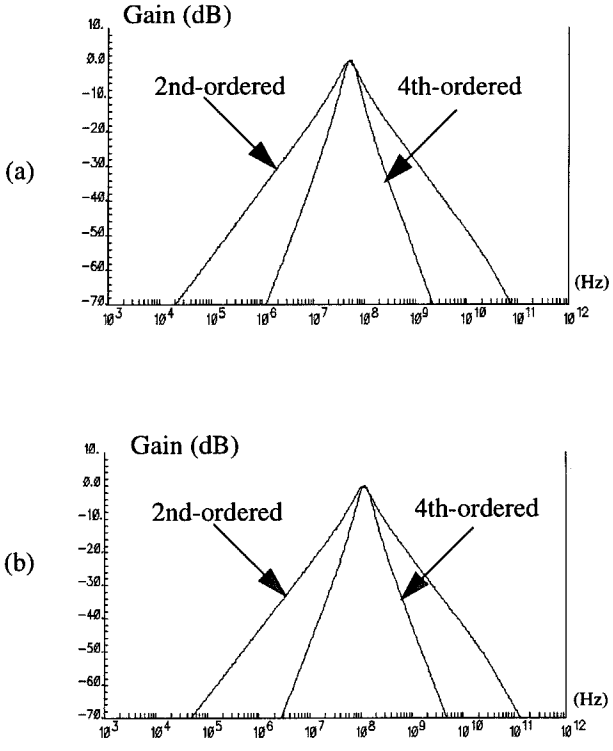

Fig.7. Comparison of the frequency response of the second-order bandpass biquad and the cascaded fourth-order bandpass filter a) V_{CC} = -V_{SS} = 1.5 V; b) V_{CC} = -V_{SS} = 2.5 V.

Acknowledgement

The authors are grateful to Valerie Bernon for providing some simulation results. They also acknowledge the funding provided by the Natural Sciences and Engineering Research Council of Canada (NSERC). Thanks also due to the Canadian Microelectronics Corporation (CMC) for providing the various design tools.

References

[1] C. -S. Park and R. Schaumann, "A High-Frequency CMOS Linear Transconductance element," IEEE Transactions on Circuits and Systems, Vol. CAS-33, No. 11, pp. 1132-1138, Nov. 1986.

[2] B. Nauta, "A CMOS Transconductance-C Filter Technique for Very High Frequencies," IEEE Journal of Solid-State Circuits, Vol. 27, No. 2, pp. 142-153, Feb. 1992.

[3] A. Assi, M. Sawan and R. Raut, "A New VCT for Analog IC Applications", The Eighth International Conference on Microlectronics, Cairo, December 1996.

[4] Jaime E. Kardontchik, "Introduction to the Design of Transconductor-Capacitor Filters", Kluwer Academic Publishers, Chapter 11, 1992.

[5] S. Szczepanski, R. Schaumann, " A Linear CMOS OTA for VHF Applications" Proc. IEEE International Symposium on Circuits and Systems, pp. 1344-1347, 1995.

[6] Y. P. Tsividis and J. O Voorman "Integrated Continuous-Time Filters" IEEE Press, New York, p 531, 1993.