A Full-Swing Bootstrapped BiCMOS Buffer

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Abstract

Bipolar circuits have high drive capability with low delay sensitivity to load while CMOS circuits have low power dissipation and high packing density. Combining both bipolar and MOS transistors on one monolithic substrate, Bipolar-CMOS (BiCMOS) circuits have high drive capability and low power dissipation at the expense of increased fabrication complexity. A major problem with conventional BiCMOS circuits is the reduced output swing due to the bipolar output transistors. This paper presents a novel BiCMOS circuit which uses bootstrapping to attain a full logic swing at the output. We present a design equation to estimate the size of the bootstrap capacitance as a function of power supply voltage. Simulations were performed using parameters from a 2.0 μm CMOS process with NPN option at supply voltages of 3.3 and 5 V. The circuit is a practical design which improves on the delay and power performance of previous bootstrapped BiCMOS inverters.

1. Introduction

For low power operation, Complementary Metal-Oxide-Semiconductor (CMOS) circuits have the advantage of nearly zero standby power dissipation. This feature, along with high packing density, makes the CMOS the top choice for VLSI applications. However, the switching speed of CMOS circuits is limited by the MOS transistors ability to drive large capacitive loads. Bipolar transistors, on the other hand, have good drive capability, but bipolar circuits have high power dissipation. Bipolar-CMOS (BiCMOS) [1,2] circuits are designed to fill the performance gap between CMOS and bipolar circuits, merging CMOS and bipolar transistors on a single monolithic structure to meet the demand of high-drive capability and low-power dissipation.

The conventional BiCMOS inverter is shown in Fig. 1(a). The variables \( V_{BE1} \) and \( V_{BE2} \) are the base-emitter junction voltages of \( Q_1 \) and \( Q_2 \), respectively. During output pulldown, the base of the pullup bipolar transistor \( Q_1 \) goes to \( V_{DD} \) and, hence, the output high voltage \( V_{OH} \) is \( V_{DD} - V_{BE1} \). During output pulldown, the base of the pulldown bipolar transistor \( Q_2 \) goes to \( V_{BE2} \) and the output low voltage \( V_{OL} \) is \( V_{BE} \). Consequently, the output swing is limited to \( (V_{DD} - V_{BE1} - V_{BE2}) \) due to the \( V_{BE} \) drops of \( Q_1 \) and \( Q_2 \). Elimination of the \( V_{BE} \) voltage drops is one of the main design issues in BiCMOS. Some of the techniques used to obtain a full rail-to-rail output swing and to reduce propagation delays are [3]:

(a) BiNMOS circuit.
(b) Feedback and shunting.
(c) Complementary and quasi-complementary circuits.
(d) Bootstrapping.
(e) Transient saturation.

We briefly describe these techniques.

The BiNMOS inverter [4] is a conventional BiCMOS inverter with the same pullup section and with the pulldown section replaced by an NMOS transistor to achieve a \( V_{OL} = V_{SS} \). In addition to unsymmetrical rise and fall times, one of the main drawbacks of BiNMOS is \( V_{OH} = V_{DD} - V_{BE} \).

Two circuits utilizing feedback and shunting to achieve a full output voltage swing are the base-emitter shunt feedback circuit [5] and the collector-emitter shunt circuit [3]. In the base-emitter circuit, the shunt elements are MOS transistors and are controlled by the output through feedback to have a high resistance at the beginning of the charging/discharging time and a low resistance at the end of the charging/discharging time. In the collector-emitter shunt BiCMOS circuit, a CMOS inverter is connected in parallel with the conventional BiCMOS inverter. The CMOS inverter has a full \( V_{DD} \) to \( V_{SS} \) logic swing while the BiCMOS inverter provides the high current drive. In both the BE-SHUNT and CE-SHUNT circuits, the output slew rate from \( V_{DD} - V_{BE} \) to \( V_{SS} \) and from \( V_{BE} \) to \( V_{SS} \) is much slower than the slew rate during the middle of the voltage transition. Thus, while successful in achieving full swing operation, these circuit techniques fail to achieve fast switching transitions, thus prompting the need for...
circuits which achieve full swing operation with faster delay.

Complementary and quasi-complementary circuit techniques used for attaining a full swing at the output have complementary bipolar transistors in the output stage [3, 6]. These circuits are successful in attaining a full logic swing at the output, but have low switching speed and require PNP and NPN bipolar transistors.

A dynamic circuit technique called bootstrapping [7] uses a feedback capacitor to couple charge from the output node on the low-to-high output transition to boost an internal node above the power supply voltage to achieve a full output voltage swing. BiCMOS circuits using bootstrapping achieve a full logic swing operating at supply voltages as low as 1.5 V [8] and outperform the quasi-complementary BiCMOS circuits in terms of delay time and power consumption at supply voltages as low as 2.5 V. Also, the performance of the circuit using the bootstrapping technique is insensitive to minor changes in process variations. A bootstrapped BiCMOS circuit operating at supply voltage as low as 1.2 V with delay performance improvement over CMOS as large as 40 - 60% has been reported [9].

For high speed switching performance, the transient saturation technique saturates the bipolar transistors only during switching periods but requires a PNP transistor. The PNP pull-up transistor is turned OFF immediately after the output reaches $V_{off}$ rather than during the high-to-low transition. In [10], a 1.5 V, full swing BiCMOS circuit using transient saturation techniques has faster delay than CMOS and Complementary BiCMOS for supply voltages as low as 1 V.

One problem with conventional BiCMOS is the bipolar output transistors limit the output voltage swing to $V_{DD} - 2V_{BE}$. To address this problem, we develop a full swing BiCMOS inverter using NPN, NMOS, and PMOS transistors (no PNP). This work develops a bootstrapping technique to boost the base voltage of the bipolar pull-up transistor to $V_{DD} + V_{BE}$, resulting in a logic high level of $V_{DD}$. The NMOS pull-down transistor produces a logic low level of $V_{SS}$. Our circuit has faster low-to-high propagation delay at large capacitive loads than previous BiCMOS circuits at 3.3 and 5 V.

The paper is organized as follows. The proposed bootstrapped BiCMOS circuit is presented in Section 2 as well as a circuit model to estimate the bootstrap capacitance to achieve a full output logic swing. Section 3 compares the delay performance and average power dissipation of the proposed circuit to other BiCMOS circuits at supply voltages ranging from 3.3 V to 5 V. Finally, Section 4 gives a summary of the work presented in this paper.

2. Proposed Bicmos Circuit Theory

This section introduces the novel BiCMOS circuit which uses bootstrapping to achieve a fast rail-to-rail output swing. First, we present a qualitative description of the circuit operation during the low-to-high and high-to-low output transitions. Second, we describe the bootstrap circuit model, the estimation of the parasitic capacitance, and the calculation of the bootstrap capacitance.

The proposed BiCMOS inverter, shown in Fig. 1(b), uses a BiCMOS configuration with a bipolar pull-up, $Q_1$, and NMOS pull-down, $M_3$. Transistors $M_1$, $M_2$, and $M_3$ are

![Fig. 1. (a) Schematic of conventional BiCMOS bootstrapping. (b) Schematic of proposed BiCMOS circuit using bootstrapping.](#)
act as a CMOS inverter to control $Q_1$. Transistor $M_2$ blocks current flowing from node 4 to $V_{DD}$. The body of $M_2$ is tied to the drain causing it to act as a diode using the body-source junction. Care should be taken to introduce guard rings to prevent latch-up. Transistor $M_4$ isolates the bootstrap capacitance $C_B$ from the base of $Q_1$ when the output is low. Transistors $M_3$ and $M_5$ precharge the bootstrap capacitance during the output low period. The parasitic capacitance, $C_p$, represents the total parasitic capacitances at nodes 4 and 6.

When the input voltage is $V_{DD}$, transistor $M_1$ is OFF and $M_3$ is ON, thus, $Q_1$ is OFF. At the same time, controlled by the input high voltage, $M_5$ is ON and operates in the linear region. Thus, $I_D$ is zero and the output low voltage is $V_{OL} = V_{SS}$. Transistor $M_5$ is turned OFF by the input high voltage and the bootstrap capacitance is isolated from the base of $Q_1$. Transistors $M_4$ and $M_5$ provide a charging path for the bootstrap capacitance from the supply rail to charge node 6 voltage to $V_{DD} - V_{OE}$. Note that the threshold voltage $V_{th}$ is large due to the substrate bias effect.

Now consider the input transition from a logic high of $V_{DD}$ to a logic low of $V_{SS}$ which turns OFF the NMOS pull-down transistor $M_5$. Controlled by the input signal, the PMOS transistor $M_1$ turns ON and NMOS transistor $M_3$ turns OFF. The bootstrap capacitance $C_B$ is now connected between the base of $Q_1$ and the output node. Also, $M_3$ turns OFF and $M_1$ turns ON, so the pull-up transistor $Q_1$ turns ON.

Once transistor $Q_1$ turns ON, the output load capacitance charges up, raising the output voltage and coupling charge from the output node to the parasitic capacitance $C_p$ on node 4. If $C_B / C_p$ is large enough, the voltage on node 4 is boosted above the supply voltage. When the base node voltage reaches $V_{DD} + V_{BE1}$, the output reaches $V_{DD}$, the desired $V_{OH}$. Thus, the circuit achieves a full rail-to-rail voltage swing at the output.

Some charge on $C_B$ is transferred to the parasitic capacitance $C_p$. Thus, choosing the right size for $C_B$ becomes an important design issue for achieving the required voltage on the base node of $Q_1$. We use a simplified circuit model to estimate the bootstrap capacitance [7]. Neglecting the base current of $Q_1$, the circuit model in Fig. 2 is used to estimate the size of the bootstrap capacitance for full swing operation of the circuit. The parasitic capacitance on the base node is $C_p$ and $v_B(t)$ is the voltage across $C_p$. The bootstrap capacitance is $C_B$ and $v_B(t)$ is the voltage across $C_B$. The output voltage is $v_{OE}(t)$.

The circuit model for $t < 0$, when $C_B$ is being precharged, is given in Fig. 2(a). Transistors $M_1$ and $M_2$ are modeled as a current source, $I$, and $M_6$ is OFF, disconnecting the bootstrap capacitance from the base node of $Q_1$. At $t = 0$, $M_6$ turns ON and the bootstrap capacitance is between the output node and the base node of $Q_1$. Transistor $M_2$, operating as a reverse-biased diode, effectively disconnects the current source from the base of $Q_1$, causing the model in Fig. 2(b) to correspond to the subsequent functioning of the circuit.

Applying KVL around the loop of Fig. 2(b),

$$v_p(t) = v_B(t) + v_{OE}(t). \quad (1)$$

Applying KCL at the base node and neglecting $i_{B1}$,

$$C_p \frac{dv_B}{dt} = -C_B \frac{dv_{OE}}{dt}. \quad (2)$$

Using (1) in (2) to eliminate $v_{OE}$,

$$-(C_B/C_p + 1)dv_B = dv_p. \quad (3)$$

Integrating the left-hand side of (3) from $v_p(0) = V_{OE} - V_{th}$ to $v_p(t) = V_{DD} + V_{BE1}$ and the right hand side from $v_p(0) = V_{OE} = 0$ to $v_p(t) = V_{OE} = V_{DD}$, and rearranging, we have

$$C_B/C_p = (V_{BE1} + V_{th})/(V_{DD} - V_{BE1} - V_{th}). \quad (4)$$

We use (4) to calculate the required value of the bootstrap capacitance $C_B$ for a given supply voltage and parasitic capacitance $C_p$. The parasitic capacitance $C_p$ is the sum of the base-emitter and the base-collector capacitances of $Q_1$, and the oxide and the junction capacitances of the MOS transistors connected to nodes 4 and 6. In all calculations, the capacitances are estimated for the worst case.

3. Performance Results

In this section, we validate the performance of our proposed BiCMOS inverter through SPICE2G6 [11] simulations and compare the performance of our circuit to the performance of previous circuits. We verify $V_{OH}$ vs. $C_B$ / $C_p$, and compare delay performance and average power.
dissipation with CMOS [7], BESHUNT [6], CESHUNT [3], and BFBiNMOS [9] inverters. The availability of a CMOS process with NPN option only has inhibited us from comparing our circuit to circuits using PNP transistors. All the simulations use the BJT and MOS transistor parameters of a 2.0 µm CMOS process with NPN option. The MOS transistors are all the same size except the NMOS output pull-down is twice as large and the PMOS pull-up in the CMOS inverter is six times as large. All the bipolar transistors are 2x1 NPNs.

We estimate the worst case parasitic capacitance, $C_p$, is 0.47 pF. From (4), we calculate the bootstrap capacitance needed for full swing operation. See Table I. We use $V_{BE} = 0.7$ V and $V_{st}$ varies with $V_{DD}$. In simulations, we use a value of $C_B$ which is 15% higher than calculated. In all simulations, $C_B$ has been implemented as an ideal capacitor. In an integrated circuit, $C_B$ could be implemented using two polysilicon layers. We estimate the bootstrap capacitance requires an area approximately equal to 42 X area of the active area of a minimum size MOS transistor. Note that $C_B$ would add about 12% of its value to the load capacitance due to parasitic capacitance between 1st layer poly and substrate.

The proposed circuit was simulated using transient analysis to verify the $V_{OH}$ value with $V_{DD} = 5$ V. The ratio $C_B / C_p$ was varied from 0 to 2.1. The $V_{OH}$ results are plotted in Fig. 3. For values of $C_B / C_p > 1.2$, $V_{OH} = 4.90$ V. As $C_B / C_p$ is decreased below 0.7, $V_{OH}$ decreases to $V_{DD} - V_{BE}$ and $C_B$ has no effect on $V_{OH}$.

We compare the delay performance of our circuit at $V_{DD} = 3.3$ V and $V_{DD} = 5$ V to the CMOS, BESHUNT, CESHUNT, and BFBiNMOS circuits using a 4 inverter chain with the load capacitance placed at the output of the third inverter. The propagation delays were measured at the third inverter with a fanout of one.

In general, at small load capacitances, the CMOS inverter had the fastest $t_{PHL}$ and $t_{PLH}$ measured at $V_{DD}/2$. Our proposed circuit had the best $t_{PHL}$ at large load capacitances, while CESHUNT and BESHUNT had the best $t_{PLH}$.

With $V_{DD} = 5$ V, $t_{PHL}$ versus load capacitance is plotted in Fig. 4(a) and the $t_{PLH}$ versus load capacitance is plotted in Fig. 4(b). The proposed circuit is labeled PROP. Consider the plot of $t_{PHL}$ versus load capacitance. The proposed circuit is about 0.4 ns slower than CMOS and 1 to 2 ns faster than the BFBiNMOS circuit for all load capacitances. The BESHUNT circuit with bipolar pull-down transistor has the best delay performance for loads above 1.6 pF.

### Table I. Bootstrap capacitance values. The last column contains the values used during the simulations.

<table>
<thead>
<tr>
<th>$V_{DD}$ (V)</th>
<th>$V_{st}$ (V)</th>
<th>$C_B / C_p$</th>
<th>$C_B$ (calc.) (pF)</th>
<th>$C_p$ (sim.) (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3</td>
<td>1.5</td>
<td>2.0</td>
<td>0.94</td>
<td>1.10</td>
</tr>
<tr>
<td>4.0</td>
<td>1.7</td>
<td>1.5</td>
<td>0.71</td>
<td>0.81</td>
</tr>
<tr>
<td>5.0</td>
<td>1.9</td>
<td>1.1</td>
<td>0.52</td>
<td>0.60</td>
</tr>
</tbody>
</table>

**Fig. 3.** $V_{OH}$ as a function of $C_B / C_p$. For small values of $C_B / C_p$, the bootstrap capacitance has little effect on $V_{OH}$. For large values of $C_B / C_p$, $V_{OH}$ is limited to $V_{DD}$. **Fig. 4.**
In the plot of $t_{PLH}$ versus load capacitance, we see that the BFBiN莫斯 circuit performs marginally better than the proposed circuit for load capacitances below 1.3 pF but is much slower at large loads. The CMOS circuit, while performing well at smaller loads, is also much slower for large loads. BESHUNT and CESHUNT circuits, although exhibiting good delay insensitivity, have larger overall delays than the proposed circuit. The proposed circuit has the best delay performance for load capacitances above 1.4 pF and exhibits good delay insensitivity to load variation.

For a supply voltage of $V_{DD} = 3.3$ V, $t_{PLH}$ versus load capacitance and $t_{PHL}$ versus load capacitance are plotted in Fig. 4(c) and Fig. 4(d), respectively. The results for $V_{DD} = 3.3$ V are qualitatively similar to the $V_{DD} = 5$ V results. Our proposed circuit is about 2.3 ns slower than CMOS on the $t_{PLH}$ delay and 4 to 13 ns faster than the BFBiN莫斯. For load capacitances above 3.8 pF, CESHUNT has the fastest $t_{PHL}$.

In the plot of $t_{PLH}$ versus load capacitance, CMOS circuit has the smallest delay for small loads. The BFBiN莫斯, BESHUNT, and CESHUNT circuits, while exhibiting good delay insensitivity to load variation, have large delays. The proposed circuit has the smallest delay for load capacitances above 2.5 pF.

We now consider the $V_{DD}$ operating range of the circuit. Consider (5). A positive denominator requires $V'_{DD} > (V_m + V_{BE})$. Therefore, for $V_m = 1.9$ V and $V_{BE} = 0.7$ V, we have $V'_{DD} > 2.6$ V. The proposed circuit achieves full voltage swing at the output for supply voltages above 2.6 V. Simulations have shown that the degradation in delay performance was large when $V_{DD}$ approaches 2.6 V. However, for lower $V_{DD}$, the threshold voltages of the MOS transistors would also be smaller than those used in this work.

The average power dissipation has been simulated at 0.5 MHz frequency with a load capacitance of 5 pF for supply
voltages of 3.3 V, 4 V, and 5 V. The results are plotted in Fig. 5. CMOS has the lowest power dissipation ranging from 9.83 to 21.1 μW. The power dissipation of the proposed circuit ranges from 0.04 to 4.3 μW above CMOS and is lower than any of the other BiCMOS circuits.

The BiCMOS circuits are compared in terms of the number of BJTs, MOS transistors, and capacitors, given in Table II. The proposed circuit uses fewer transistors compared to the other bootstrapped BiCMOS circuit.

4. Summary

BiCMOS merged the low power dissipation and high packing density features of MOS circuits with the high drive capability of bipolar circuits. One problem associated with BiCMOS circuits is the voltage swing loss at the output. In this paper, we proposed a BiNMOS inverter circuit which uses a novel bootstrapping configuration to achieve a full swing at the output. A bootstrap capacitance couples charge from the output node on the low-to-high output transition to boost an internal node above the power supply voltage. Our circuit meets the design objective of a full logic swing at the output. In addition, the proposed circuit has fewer transistors and simpler operation than a previously reported BiCMOS circuit using bootstrapping. Delay performance comparisons were done at supply voltages of 3.3 V and 5 V. The proposed circuit has $t_{pUL}$ delay slightly higher than the CMOS inverter for all loads and has faster $t_{PLH}$ delay than CMOS and three other BiCMOS circuits at large loads. The average power dissipation at 3.3 V, 4 V, and 5 V supply voltages is slightly higher than the CMOS circuit and lower than the other BiCMOS circuits.

References


Table II. Number of devices used in BiCMOS inverters.

<table>
<thead>
<tr>
<th>Inverter</th>
<th>BJT</th>
<th>MOST</th>
<th>Capacitors</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMOS</td>
<td>0</td>
<td>2</td>
<td>0</td>
</tr>
<tr>
<td>BESHUNT</td>
<td>2</td>
<td>7</td>
<td>0</td>
</tr>
<tr>
<td>CESHUNT</td>
<td>2</td>
<td>6</td>
<td>0</td>
</tr>
<tr>
<td>BFBiNMOS</td>
<td>1</td>
<td>11</td>
<td>1</td>
</tr>
<tr>
<td>PROP</td>
<td>1</td>
<td>7</td>
<td>1</td>
</tr>
</tbody>
</table>