FPGA ‘97

1997 ACM Fifth International Symposium on Field-Programmable Gate Arrays

February 9-11, 1997
Monterey Beach Hotel
Monterey, California USA

FPGA ‘97 is sponsored by the ACM Special Interest Group on Design Automation (SIGDA) with support from Altera Corp., Xilinx Inc. and Actel Corp.
Welcome to the 1997 ACM/SIGDA International Symposium on Field Programmable Gate Arrays (FPGA'97). This annual symposium is the premier forum for presentation of advances in all areas related to the FPGA technology, and also provides a relaxed atmosphere for exchanging ideas and stimulating discussions for future research and development in this exciting new field.

This year's symposium sees a strong increase of interest in the FPGA technology, with over 20% increase in paper submissions. The technical program consists of 20 regular papers, 35 poster papers, an evening panel, and an invited session. The technical papers present the latest results on advances in FPGA architectures, new CAD algorithms and tools for FPGA designs, and novel applications of FPGAs. The Monday evening panel presents the debate if reconfigurable computing is commercially viable. The invited session on Tuesday morning addresses the challenges for architecture development, CAD tools, and circuit design of one million-gate FPGAs and beyond.

We hope that you find the symposium informative, stimulating, and enjoyable.

Carl Ebeling  
General Chair

Jason Cong  
Program Chair
Organizing Committee

**General Chair:** Carl Ebeling, University of Washington  
**Program Chair:** Jason Cong, UCLA  
**Publicity Chair:** Scott Hauck, Northwestern University  
**Finance Chair:** Jonathan Rose, University of Toronto  
**Local Chair:** Pak Chan, UC Santa Cruz

Programming Committee

<table>
<thead>
<tr>
<th>Michael Butts, Quickturn</th>
<th>Pak Chan, UCSC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Jason Cong, UCLA</td>
<td>Carl Ebeling, U. Washington</td>
</tr>
<tr>
<td>Masahiro Fujita, Fujitsu Labs.</td>
<td>Scott Hauck, Northwestern Univ</td>
</tr>
<tr>
<td>Dwight Hill, Synopsys</td>
<td>Brad Hutchings, BYU</td>
</tr>
<tr>
<td>Sinan Kaptanoglu, Actel</td>
<td>David Lewis, U. Toronto</td>
</tr>
<tr>
<td>Jonathan Rose, U. Toronto</td>
<td>Richard Rudell, Synopsys</td>
</tr>
<tr>
<td>Rob Rutenbar, CMU</td>
<td>Gabriele Saucier, Imag</td>
</tr>
<tr>
<td>Martine Schlag, UCSC</td>
<td>Tim Southgate, Altera</td>
</tr>
<tr>
<td>Steve Trimberger, Xilinx</td>
<td>Martin Wong, UT Austin</td>
</tr>
<tr>
<td>Nam-Sung Woo, Lucent Technologies</td>
<td></td>
</tr>
</tbody>
</table>

Acknowledgments

The organizing committee would like to thank Lisette Burgos from ACM and Debbie Hall from Meeting Hall, Inc. for assisting the symposium organization and making detailed arrangements. Jie Fang and Yeanyow Hwang from UCLA helped a great deal in collecting paper submissions and reviews, communicating with the authors, and assembling the final proceedings. Their effort are also very much appreciated.
# Table of Contents

## Session 1: FPGA Architectures
**Session Chair:** Rob Rutanbar, Carnegie Mellon University

1.1. Architecture Issues and Solutions for a High-Capacity FPGA, ........................................3  
   S. Trimberger, K. Duong, B. Conn, Xilinx, Inc.

1.2. Memory-to-Memory Connection Structures in FPGAs with Embedded Memory Arrays,  
    Steven J.E. Wilton, University of British Columbia, J. Rose, Z.G. Vranesic, University of Toronto

1.3. Laser Correcting Defects to Create Transparent Routing for Large Area FPGAs,  
    G.H. Chapman, B. Dufort, Simon Fraser University

## Session 2: FPGA Partitioning and Synthesis
**Session Chair:** Richard Rudell, Synopsys, Inc.

2.1. I/O and Performance Tradeoffs with the FunctionBus during Multi-FPGA Partitioning,  
    F. Vahid, University of California, Riverside

2.2. Partially-Dependent Functional Decomposition with Applications in FPGA Synthesis and Mapping,  
    J. Cong, Y. Hwang, Univ. of California, Los Angeles

2.3. General Modeling and Technology-Mapping Technique for LUT-based FPGAs,  
    A. Chowdhary, J.P. Hayes, University of Michigan

## Session 3: Rapid Prototyping and Emulation
**Session Chair:** Carl Ebeling, Univ. of Washington

3.1. The Transmogrifier-2: A 1 Million Gate Rapid Prototyping System,  
    D.M. Lewis, D.R. Galloway, M. V. Ierssel, J. Rose, P. Chow, University of Toronto

3.2. Signal Processing at 250 MHz using High-Performance FPGA’s,  
    B. V. Herzen, Rapid Prototypes, Inc.

3.3. Module Generation of Complex Macros for Logic-Emulation Applications,  
    W. J. Fang, C.H. Wu, D.P. Chen, Tsinghua Univ.

## Session 4: Reconfigurable Computing
**Session Chair:** Jonathan Rose, Univ. of Toronto

4.1. Wormhole Run-time Reconfiguration,  
    R. Bittner, P. Athanas, Virginia Polytechnic Institute

4.2. Improving Functional Density Through Run-Time Constant Propagation,  
    M.J. Wirthlin, B.L. Hutchings, Brigham Young University

4.3. YARDS: FPGA/MPU Hybrid Architecture for Telecommunication Data Processing,  
Evening panel: Is Reconfigurable Computing Commercially Viable? .........................101

Session 5: FPGA Floorplanning and Routing
Session Chair: Dwight Hill, Synopsys, Inc.

5.1. Synthesis and Floorplanning for Large Hierarchical FPGAs, ...............................105
      H. Krupnova, C. Rabedaoro, G. Saucier, Institut National Polytechnique de
      GrenobleCSI
5.2. Performance Driven Floorplanning for FPGA Based Designs, ..............................112
      J. Shi, D. Bhatia, University of Cincinnati
5.3. FPGA Routing and Routability Estimation Via Boolean Satisfiability, ....................119

Session 6: Challenges for One Million-Gate FPGAs and Beyond
Session Chair: Jason Cong, Univ. of California, Los Angeles

6.1. Architectural and Physical Design Challenges for One Million Gate .................129
      FPGAs and Beyond, J. Rose, University of Toronto and D. Hill, Synopsys, Inc.
6.2. Challenges in CAD for the One Million Gate FPGA, ..........................................133
      K. Keutzer, Synopsys, Inc.

Session 7: Studies of New FPGA Architectures
Session Chair: Steve Trimberger, Xilinx, Inc.

7.1. A CMOS Continuous-time Field Programmable Analog Array, ..........................137
      C.A. Looby, C. Lyden, National Microelectronics Research Center
7.2. Buffer Minimization and Time-multiplexed I/O on Dynamically ........................142
      Reconfigurable FPGAs,
      D. Chang, M. Marek-Sadowska, Univ. of California, Santa Barbara
7.3. Generation of Synthetic Sequential Benchmark Circuits, .................................149
      M. Hutton, J. Rose, D. Corneil, University of Toronto

Session 8: Novel Design and Applications
Session Chair: Pak Chan, Univ. of California, Santa Cruz

8.1. Synchronous Up/Down Binary Counter for LUT FPGAs with ............................159
      Counting Frequency Independent of Counter Size,
      A.F. Tenca, M. D. Ercegovac, Univ. of California, Los Angeles
8.2. A FPGA-based Implementation of Fault-Tolerant Neural ................................166
      Architecture for Photon Identification, M. Alderight, E.L. Gummati, V. Piuri, G.R.
      Sechi, Consiglio Nazionale delle Ricerche, Universita degli Studi di Milano, Politecnico
      di Milano
Monday Evening Panel

Is Reconfigurable Computing Commercially Viable?

Moderator: Herman Schmit, Carnegie Mellon Univ.

In order to be commercially viable, an FPGA-based solution to a computational problem must have lower cost than a solution based on a microprocessor, or a solution based on a custom or semi-custom ASIC. Conventional FPGAs never have higher performance than a comparable ASIC on a single application, and are unlikely to ever be as ubiquitous and generic as microprocessors. Therefore, FPGAs may be limited to markets where there is not enough volume to justify the design of an ASIC, and where the performance needs of the application cannot be met by an ISP. How big is this market? Do "killer-applications" that fit these constraints really exist?

An FPGA implementation does have one advantage over the ASIC solution: reconfigurability. A FPGA-based accelerator could, at different times, accelerate one of innumerably many possible applications. So rather than one "killer-application" perhaps there are thousands of little applettes, whose performance can be significantly accelerated using an FPGA-based system. Reconfigurable hardware systems also have many of the same advantages as microprocessor-based systems, such as upgradeability, standardization of platforms, and amortization of development costs.

In this panel session, we will try to address the questions of whether there will be a mass-market for FPGA-based computing solutions. Are there large sets of applications whose performance requirements far exceed that offered by microprocessors but which are only occasionally executed? Where are these applications? Does the ability to reconfigure during execution change the cost and performance benefits of reconfigurable hardware significantly? What are the key challenges to making reconfigurable computing a reality, and what can PLD manufacturers, system houses, government, and academia do to overcome these obstacles?

Panelists:

Steve Casselman: President, Virtual Computer Corp.
Daryl Eigen: President, Metalithic Systems, Inc.
Robert Parker: Deputy Director, ITO, DARPA
Peter Athanas: Assistant Professor, Virginia Polytechnic Institute
Robert Colwell: Pentium Pro Architecture Manager, Intel Corp.
Author Index

M. Alderighi 166
P. Athanas 79
D. Bhatia 112
R. Bittner 79
D. Chang 142
G.H. Chapman 17
D. Chen 69
P. Chow 53
A. Chowdhary 43
J. Cong 35
B. Conn 3
D. Corneil 149
B. Dufort 17
K. Duong 3
M. D. Ercegovac 159
W. Fang 69
D.R. Galloway 53
E.L. Gummati 166
J.P. Hayes 43
B. V. Herzen 62
D. Hill 129
B.L. Hutchings 86
M. Hutton 149
Y. Hwang 35
M. V. Ierssel 53

K. Keutzer 133
H. Krupnova 105
D.M. Lewis 53
C.A. Looby 137
C. Lyden 137
M. Marek-Sadowska 142
T. Miyazaki 93
V. Piuri 166
C. Rabedaooro 105
J. Rose 10, 129, 53, 149
R.A. Rutenbar 119
G. Saucier 105
H. Schmit 101
G.R. Sechi 166
J. Shi 112
A.F. Tenca 159
S. Trimberger 3
A. Tsutsui 93
F. Vahid 27
Z.G. Vranesic 10
S. Wilton 10
M.J. Wirthlin 86
R.G. Wood 119
A.C. Wu 69
Session 1: FPGA Architectures
Session 2: FPGA Partitioning and Synthesis
Session 3: Rapid Prototyping and Emulation
Session 4: Reconfigurable Computing
Session 5: FPGA Floorplanning and Routing
Session 6: Challenges for One Million-Gate FPGAs and Beyond
Session 7: Studies of New FPGA Architectures
Session 8: Novel Design and Applications