Design of Partially Parallel Scan Chain

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Abstract

This paper presents a design-for-testability technique, called partially parallel scan chain (PPSC), which aims at reduction of test length for sequential circuits. Since the partially parallel scan chain allows to control and observe subset of flip-flops (FFs) concurrently during scan shift operations, the number of scan shift clocks is reduced.

1. Introduction

In PPSC, some FFs are arranged in parallel and some FFs are in serial. Since the FFs arranged in parallel can be controlled and observed concurrently, the number of scan shift clocks is reduced. Although a subset of states can not be set by scan shift operations, the proposed method can detect all the sequentially detectable faults. PPSC requires only one scan input line and one scan output line, thus it is different from parallel scan methods[1]. Moreover PPSC reuses the original function for its construction as much as possible.

2. Configuration of PPSC

Parallel FFs in PPSC are found in particular subcircuits. In this paper, four types of subcircuit are presented and the configurations of PPSC are described related to the subcircuits. In Fig.1, the thin solid lines denote an original subcircuit, and the thick solid lines from parallel scan methods[1]. Moreover PPSC reuses the original function for its construction as much as possible.

3. Experimental result

We experimented for ISCAS '89 benchmark circuits. Table 1 shows the results. The test length is calculated by

\[ L = n \times (v + 1) + v + 1 \]

where \( n \) is the number of scan shift clocks or FFs and \( v \) is the number of test vectors. Columns "serial" show the results of case that all FFs are arranged in serial. Columns "PPSC" show the results of the proposed method. It is found that PPSC achieves short test lengths.

\[ (0,\ldots,0) \text{ and } (1,\ldots,1) \text{ can be set and only FF } \alpha_1 \text{ can be observed. Faults which require the other states are sequentially undetectable.} \]

[Type-2] When some FFs drive a same gate, these FFs can be arranged in parallel as shown in Fig. 1(b). Note that the black filled gate is added to observe the two FFs concurrently. The faults which require state (0, 1) or (1, 0) for their detections are sequentially undetectable except for faults on \( z_1 \text{ and } z_2 \text{. Stuck-at one fault on } z_1 \text{ and } z_2 \text{ can be tested as follows. First, an input vector applied so that state (0, 1) or (1, 0) is set. Next, scan shift operation is performed. Then the fault is activated and its effect is scanned out.} \]

[Type-3] In subcircuit of Fig. 1(c), gate \( g_1 \text{ and } g_2 \text{ can be united into one gate by De Morgan’s law and the associative law. The FFs in such a subcircuit can be arranged in parallel. The black filled gate is added in order to make the signals of } z_3 \text{ inactive during scan shift operations.} \]

[Type-4] When there are three FFs which are driven by the two lines \( x_1 \text{ and } x_2 \), PPSC is configured as shown by thick solid lines in Fig. 1(d). In this subcircuit, FF \( \alpha_3 \) is not necessary to be independently controlled and observed.

Table 1 Experimental results

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<th>Circuit</th>
<th>Serial test vector</th>
<th>Serial test length</th>
<th>Scan shift clock test vector</th>
<th>Scan shift clock test length</th>
<th>PPSC test vector</th>
<th>PPSC test length</th>
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