Compact Structural Test Generation for Analog Macros

Victor Kaal and Hans Kerkhoff
MESA Research Institute
University of Twente, P.O. Box 217, 7500 AE Enschede, The Netherlands
E-mail : V.Kaal@el.utwente.nl

Abstract

A structural, fault-model based methodology for the generation of compact high-quality test sets for analog macros is presented. Results are shown for an IV-converter macro design. Parameters of so-called test configurations are optimized for detection of faults in a fault-list and an optimal selection algorithm results in determining the best test set. The distribution of the results along the parameter-axes of the test configurations is investigated to identify a collapsed high-quality test set.

1 Introduction

Nowadays, digital IC test generation is a fully automated, fault-model oriented fast process. Analog as well as mixed-signal (functional) IC test development generally requires a time-consuming, manual effort. Structural fault-model based test generation for analog macros in mixed-signal ICs has been recognized as a promising alternative or addition to cope with today's time-to-market and high quality demands [1]. However, hardly any work has been published on the automated generation of high-quality test signals for these ICs.

Inductive fault analysis (IFA) has been used to construct fault dictionaries for macros, which model the most important non-global production-caused faults to test for [2]. Using this, the high-quality requirements demanded nowadays can be met and possibilities for implementing more structured frameworks for the generation of tests for analog and mixed-signal ICs are opened [3].

This paper presents a methodology for the automatic generation of high-quality tests for analog macros, driven by a dictionary of modeled faults. This dictionary can be generated by IFA, but for simplicity we used an exhaustive list of bridging and pin-hole faults in the circuit. The definitions and methodology are illustrated by evaluating an IV-converter macro design. The test generation problem is considered to be the optimal selection of a large number of tests originating from a limited number of "seed" test configurations. A two-step approach will be used. First, for each fault in the list a test solution will be generated tailored to optimal detection of the fault-type at the indicated location. For the second step, a methodology will be shown which collapses the set of unique optimized test solutions onto a much smaller set. The collapse algorithm includes extraction and verification of shared properties of tests, based on the construction of test description used in the first step.

2 Optimal test definition

In our methodology, an optimal test solution is to be generated for the detection of each modeled fault in the fault dictionary. It must however first be defined what is exactly meant by generation and optimality of a test.

2.1 Test construction

The complete generation of wave-forms combined with automatic control / observe node selection dedicated to observability of a fault in an analog circuit is difficult. On the other hand, the selection of tests out of a predefined set of tests does not provide the possibility to tailor a test towards detection of faults. In this case, the responsibility for actual test generation is returned to the test engineer, who faces the tedious task to guarantee high fault detection with the predefined test set provided.

In our test generation methodology, we introduce *test configuration descriptions* as the solution of the mentioned problem. Figure 1 shows an example of a test configuration description that is used for our IV-converter macro example. A test configuration description dictates which nodes have to be controlled and observed. It also provides the description of the wave-forms to be applied at the control-nodes.

ED&TC '97 on CD-ROM

Macro type:	IV-converter
Test configuration:	Step response 1
Input nodes:	Iin
Output nodes:	Vout
Test parameters:	**Base**, **Elev** (dc current values)
Variables:	sl, sa, t
Description: *in*	I(Iin) = step(**Base**,**Elev**,slew-rate=sl)
return value	ΣV(Vout); sample-rate=sa, test-time=t

Figure 1: A test configuration description example which is used for the IV-converter.

Furthermore, it describes any post-processing on measurements on the observation-nodes, resulting in the *return value(s).* In figure 1, a step-shaped input current is described using the *test parameters* 'base', 'elev' and the *variable* 'sl'. This signal should be applied to the node named 'Iin'. The voltage of the output node 'Vout' should be sampled and accumulated during the test time. Variables 'sa' and 't' are used to denote required sample rates and test time. Sets of test configuration descriptions are shared by macro types, i.e. for macros of the IV-converter type, figure 1 provides a general framework for description of one test. Node names should however be standardized. The concept is designed to support the reusability of the work of a test engineer.

In a *test configuration implementation* the general description is further specified for an individual macro. Boundary values for the test parameters and values for the variables are added to the description, provided by e.g. the test engineer. A test can be regarded as being built up from a test configuration implementation (test configuration from now on) and attached test parameter values. This definition of a test enables automated calculation of test parameter values optimized for detection of the fault-type at a specific location.

2.2 Test optimization

The base for the generation algorithm is given by providing a description of our criteria used for the optimization of test parameters and the selection of test configurations.

At the macro-level, a fault can only be detected if between the faulty macro responses on the one hand, and any non-nominal behavior on the other, a difference can be monitored with the available test equipment. The concept of *tolerance-boxes* has been frequently used in literature [4] [5]. This is a means to construct a window in measurement space which safely boxes in expectable response values based on known variations on process parameters. In this paper we also include the accuracy specifications of test equipment, as it would be useful to construct an envelope which boxes in an area where fault-detection can not be guaranteed.

Given a specific fault, a sub-set of test configurations is potentially suited for detection purposes. For such configurations, regions in the allowed test-parameter space can be identified which enable detection. Based on this data it is very hard to pick out the best suitable test configuration with attached parameter values. Among the options are the use of distance values relative to nominal or deviation values. However, what do they indicate if test configurations are to be ranked with respect to detectability?

Fault impact is an essential part of our definition of optimal tests. The impact of a fault reflects the physical size of the actual defect, represented by a fault model parameter value set. In the case of a bridging fault, the associated model parameter "resistance" can be increased to weaken the impact and decreased for intensification of the impact. Our definition of the optimal test for a specific fault is the test which is still able to detect the fault at the specified location if the impact of the fault is weakened, even to such extend that all other parameter combinations and test configurations fail. We will refer to this level of impact as the *critical impact level*.

As a consequence, the generation comes up with a solution suited for detection of the type of fault instead of the exact specified fault in the fault dictionary. This enables collapsing of dictionaries, but may in some cases result in a test which masks the specified fault. Based on the experiments with the IV-converter, the latter seems not very likely to occur although hard to generally prove. The definition of optimality can be extended for faults which have an undetectable impact. Instead of ignoring such faults, it is possible to improve resulting quality by increasing the impact until detection does occur at the most sensitive test. The inclusion of this *fault-impact manipulation* only slightly influences generation times.

Selecting the most appropriate test for a fault is heavily relying on the model parameter values of the fault used. It will be shown that test generation by using a *fixed* predefined set of possible tests to select from, and detection of fault models as plain evaluation criterion, will not result in the most sensitive test set to detect the fault types indicated by the fault list. Therefore, high-quality test sets require test generation which goes beyond simple selection strategies and includes automated tailoring towards optimal detection of specified faults. Though it may seem hard to fully automate the generation of tests for analog macros, a predefined set of promising tests could be used as general *seed* values for the generation of tests. In line with our approach of test construction, a seed value consists of both a test configuration and a particular test parameter set implementation. This limited collection of seed test values is to be provided by e.g. the designer, leaving the selection and test-signal optimization to our automatic test-generation software.

3 Test generation

In this section fault-specific test generation is covered. An efficient algorithm is presented which optimizes test-parameters in test configurations for the detection of a fault and selects the best combination. Results are shown for an IV-converter macro.

3.1 Test sensitivity analysis

Basically the most sensitive test for the detection of a modeled fault has to be found. As shown later, an algorithm is available which optimizes test parameters in a test configuration. Figures 2,3,4 show so-called **t**est-**p**arameter **s**ensitivity (tps-)graphs for a specific fault with regard to type and location.

In the example of figures 2,3,4, a trans-harmonic distortion (THD) is the return value of the test configuration, hosting tests to detect a resistive short (bridging fault) of decreasing impact (R=10, 34 and 75 kΩ) between two arbitrarily chosen nodes in the IV-converter macro. Along the axis run the attached test parameters subject to optimization, which are in these examples the DC-level 'Iin_{dc}' and the frequency 'freq(Iin)' of the sine-wave shaped input current.

Tps-graphs reflect the parameter sensitivity in a particular way, which is described by the following definition. A specific test is defined by a **t**est **c**onfiguration tc and a parameter value set T_{tc}. In figures 2,3,4, T_{tc} is an implementation of the transposed test parameter set $[Iin_{dc}, freq(Iin)]^T$. Application of a test to an arbitrary macro, results in the p **r**eturn values $[\mathbf{r}_1(T_{tc})\ldots\mathbf{r}_p(T_{tc})]^T$ denoted by $\mathbf{R}(T_{tc})$. For the examples, $R(T_{tc})$ is the THD value. In the fault-free macro case, $R(T_{tc})$ is within the tolerance box values $[r_{\sigma,1}(T_{tc})\ldots r_{\sigma,p}(T_{tc})]^T$ around the nominal return values $[r_{\mu,1}(T_{tc})\ldots r_{\mu,p}(T_{tc})]^T$. Figure 5 shows an example with p=2, depicting the tolerance box values, nominal values and two return value sets for the same T_{tc} vector. $R(T_{tc})_1$ may originate from either a faulty or a fault-free macro,

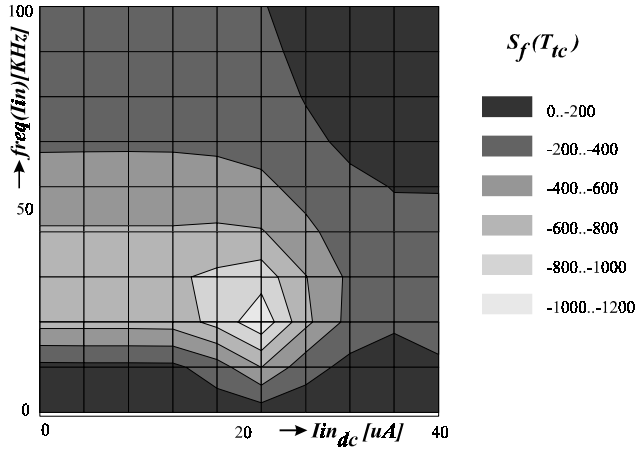

Figure 2: A tps-graph for a resistive short modeled by a 10KΩ bridge resistance, describing a THD measurement for IV-converter macros.

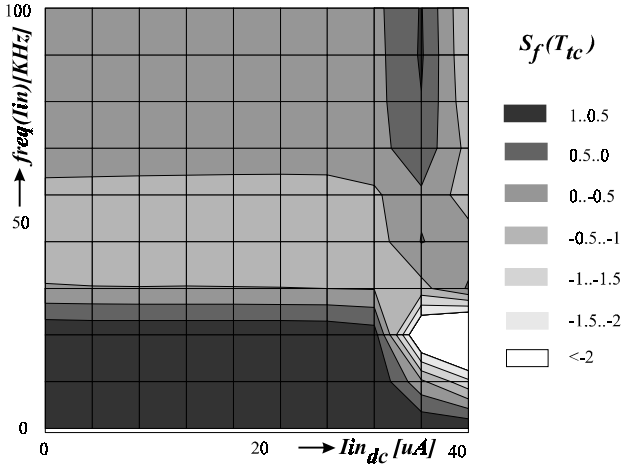

Figure 3: The tps-graph when the impact of the model is lowered to 34KΩ. Compare fig. 2.

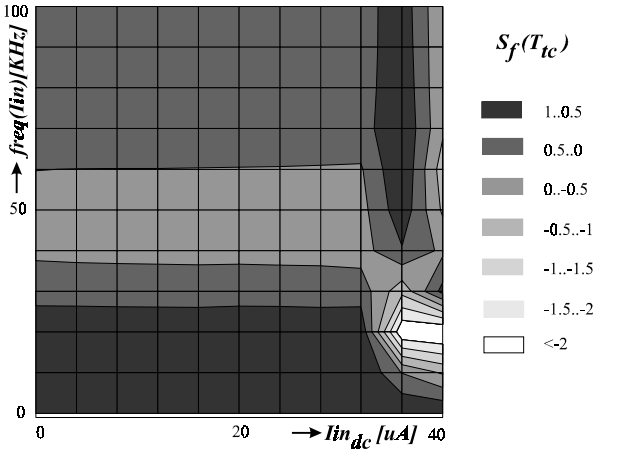

Figure 4: The tps-graph when the impact of the model is lowered to 75KΩ. Compare fig. 2.

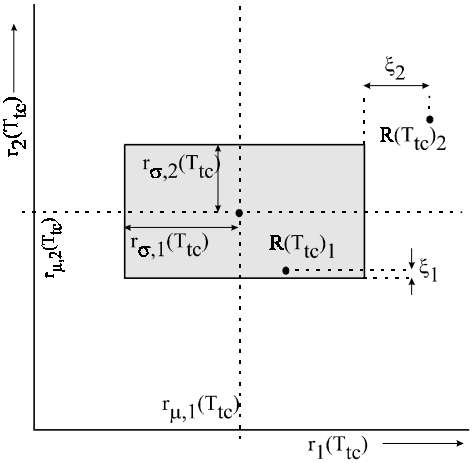

Figure 5: Visualization of 2 return values, depicted with according (gray) tolerance box and nominal values.

$R(T_{tc})_2$ can only be resulted by a faulty circuit. Simulation of a faulty circuit, in which the **f**ault model implementation **f** is inserted, while applying T_{tc}, results in the simulated return value set $R_{\mathbf{f}}(T_{tc})$. Shown in the tps-graphs is the sensitivity S_f of test parameter combinations T_{tc} for detection of the fault model f. In the single return value case $S_f(T_{tc})$ is defined as:

$$S_f(T_{tc}) = \frac{r_{\sigma,1}(T_{tc}) - |r_{f,1}(T_{tc}) - r_{\mu,1}(T_{tc})|}{r_{\sigma,1}(T_{tc})}$$

Hence, a tps-graph shows *positive* values for test-parameter regions where fault models are classified *undetectable* while *negative* values indicate regions where *detection* will occur. Selection of the minimal sensitivity value for all individual return values can be used for extension to p return value cases. In figure 5, $S_{f1}(T_{tc})_1$ and $S_{f2}(T_{tc})_2$ are $|\xi_1|/r_{\sigma,2}(T_{tc})$ and $-|\xi_2|/r_{\sigma,1}(T_{tc})$ respectively. The definition of S_f is very suitable as cost function for minimization algorithms and is used as such in our test generation algorithm. A good optimization algorithm converges to the lowest point in our two test-parameter case, the optimized test parameters values are freq(Iin)=20kHz and Iin,dc=40μA as can be seen in figure 4. The range of the parameter values shown along axis in figure 2,3,4 is determined by the specifications of the macro and the test equipment. Generally, these *constraints* must be determined and obeyed by the minimization algorithm used.

3.2 Fault impact and optimization

It can be shown, when shifting from high-impact to low-impact fault model parameter values, that tps-graphs can be classified into two categories. For high-impact modeled faults, the shape of the tps-graph is very much determined by the exact model-parameter values. We classify this as the *hard-fault tps region* of the fault impact. However, shifting towards low-impact fault models, the shape of tps-graphs becomes stable. Only a global flattening and upward shift of values will occur during further lowering of the impact of the fault model. The impact region causing such behavior will be classified as the *soft-fault tps region*. Figures 3 and 4 show two tps-graphs for a fault modeled in its soft-fault tps region for the applied test configuration. Figure 2 shows the tps-graph when the fault model has an impact somewhere in its hard-fault tps region.

When the tps-graph becomes stable for faults located in soft-fault tps-regions, the optimal test-parameter value set is found at a stable location in the tps-graph. This is shown in figures 2 and 3. During the study of the IV-converter this general observation was experienced for all bridging type and most pinhole type of faults. Sometimes test configurations proved to be insensitive for modeled faults. The effort to calculate the best test can be reduced considerably when this observation is combined with the definition of an optimal test. We assume the fault modeled at the critical impact level is in the soft-fault tps region. Then optimization over the allowed parameter space for any low-impact modeled fault version of a fault returns a test parameter value set close to the optimal one for the type of fault and test configuration. Though this conclusion can only be claimed to hold for the IV-converter and fault models used, it is expected to be far more generally applicable.

3.3 Test generation algorithm

Based on the previous observations, a much more efficient version of the algorithm presented in [6] can be constructed. Figure 6 shows the basic data flows required in this scheme for the generation of a test for one fault.

Initially, a set of test configuration descriptions and a dictionary of modeled faults is available. Furthermore, for each test configuration parameter, a seed-value and constraint values have been determined. Also, a function is available for each test configuration, estimating the tolerance box value(s) for any parameter value set.

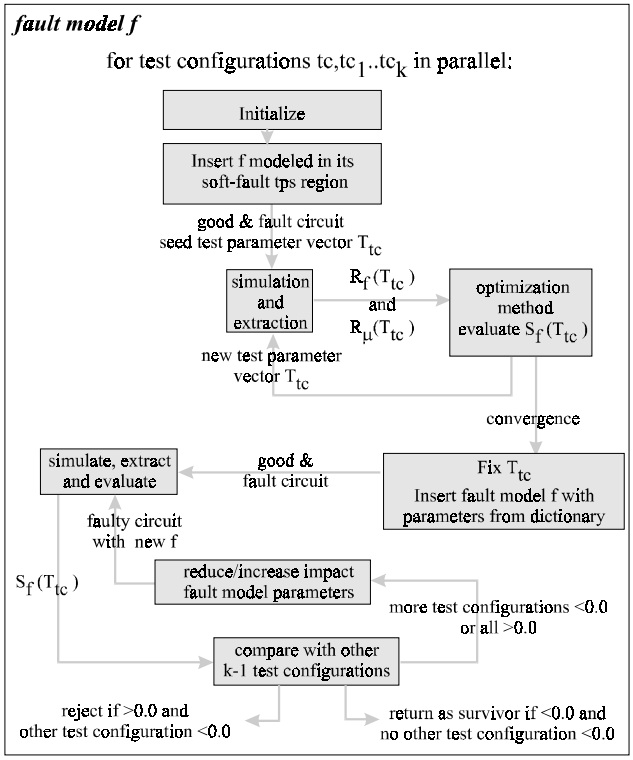

Figure 6: Scheme for the test generation for an element in the fault dictionary.

ID test configuration tc	type of test	observe node	T_{tc}	$r_{f,1}(T_{tc})$, $r_{\mu,1}(T_{tc})$	stimuli(T_{tc})
#1	DC	Vout	$I_{in,DC}$	V(Vout)	$I_{in} = I_{in,DC}$
#2	DC	Vdd	$I_{in,DC}$	I(Vdd)	$I_{in} = I_{in,DC}$
#3	transient	Vout	$[I_{in,DC}$, freq$]^T$	THD(V(Vout)(t))	I_{in} = sin($I_{in,DC}$,5μA,freq)
#4	transient	Vout	$[$base , elev$]^T$	Max(ΔV(Vout)(t))	I_{in} = PWL(t=0, base, t=10ns, base+elev, t=∞, base+elev)
#5	transient	Vout	$[$base , elev$]^T$	Σ(Δ(Vout)(t))	I_{in} = see #4

Table 1: Test configuration definitions used for the IV-converter design.

After initialization, for each fault f an optimization algorithm is started up, minimizing the cost function $S_f(T_{tc})$ for k test configurations tc, $tc_1 \ldots tc_k$. A low-impact fault model version of the fault to test for is automatically inserted in the circuit description for each test configuration. A circuit simulator is used by the minimization algorithm to find the optimal test parameter value set which shows best sensitivity.

Finally, the most sensitive test must be selected out of the k tests T_{tc} as the optimization has been carried out for each test configuration. First is started with the model in the fault list. If more than one of the tests does detect the model, the impact of the model is relaxed. If no test does detect the model, its impact is increased. The factors of decrement and increment are such that the algorithm converges to one test solution. This solution is the best test for the modeled fault.

The presented algorithm is implemented in ANSI-C and runs on an HP700 workstation. Optimizations of single-parameter test configurations are using Brent's method [7]. Multi-parameter test configurations are optimized by Powell's method described in [8], in which Brent's method is used to explore one-dimensional search-directions. Both algorithms are local optimization methods which may end up in local minima. Global optimization however requires a much larger amount of simulations which we consider unacceptable. All simulation data has been analyzed automatically and is provided by using the circuit simulator HSPICE.

3.4 Results

A CMOS IV-converter macro design has been selected for evaluation purposes [9]. In this experiment, we have confined ourselves to bridging and pinhole type of defects. The bridging type of defects are modeled by a resistor between nodes. For the pinhole type of defects, the modeling proposed by Eckersall ea. has been adopted [10] and is shown in figure 7. They conclude that defects positioned near the drain region have relative low detectability. To avoid problems with the modeling of MOS transistors related to undersized channel-lengths, we have supposed defects to be located at 25% of the channel-length from the drain. A resistance value is used

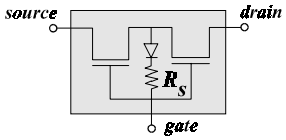

Figure 7: The pinhole fault type model

in both models to tune the impact of the model. An exhaustive list of modeled faults in the IV-converter has been created resulting in a fault list containing 55 faults. All 45 bridging faults are modeled with an initial impact of 10KΩ. The shunt-resistor R_s (figure 7) in the remaining 10 pinhole models has the initial value of 2KΩ.

Five test configurations have been selected as promising test methodologies. Two test configurations have only one attached parameter, the other three configurations have two parameters. The algorithm will find a unique test configuration and parameter value set combination as the best test for each fault in the fault list. All test configurations are described in Table 1. Say, γ is a single value originating from (processed) simulation results. Then Δγ used in the table denotes the difference between γ obtained simulating with the faulty and nominal circuit, γ_f-γ_μ. Furthermore, the function Max(γ_1,γ_2..γ_n) selects the maximum value γ_x out of the n single values $\gamma_1 \ldots \gamma_n$. Test configuration implementation #3 prescribes the transient voltage measured at Vout to be sampled at a rate and for a time as required for calculation of the THD. Test configurations #4 and #5 prescribe Vout to be sampled at 100MHz during 7.5 μs.

Constraint values (section 3.1) have been determined for all test parameters, enclosing feasible values applicable for testing the IV-converter. Furthermore, for each test configuration so-called *box-functions* have been determined estimating the (single) tolerance-box value given a test parameter value set within the allowed range. The tolerance-boxes are partially built up from the deviation expectations as function of test parameters. For the experiment with the IV-converter global and local Gaussian distributed error values have been added to the width value of each transistor. This part of box-functions is constructed using a grid over the parameter space and studying the spread in response values at each gridpoint. Furthermore, threshold values accounting for the limited

ID test configuration tc	fault type and number of faults	
	bridge(45)	pinhole(10)
#1	22	1
#2	4	3
#3	17	3
#4	-	-
#5	2	-

Table 2: The number of times a test configuration hosts the most sensitive test for a fault, sub-devised by fault type

resolution of measurement equipment have been assumed and incorporated in the box-functions.

The algorithm produced unique tests for 52 modeled faults. Three modeled faults of the pinhole type where fully insensitive for the test configurations applied. Table 2 shows for each test configuration the number of faults for which the test configurations survives as best test option. The table also provides data about the type of these faults. Test configuration #4 never appeared as host of the most sensitive test. Table 2 indicates that the resulted best tests are not homogeneously distributed over test configurations. The same can be concluded when studying the spread over the parameter spaces of the configurations which will be covered in more detail in section 4. For the one-dimensional optimization problems in our example, typically 12 evaluations of the cost function S_f where necessary. Requiring typically 130 evaluations, two-dimensional optimizations proved to be much more CPU-intensive. Each evaluation includes a simulation of the faulty and the nominal circuit.

4 Test compaction

In the previous section, a test generation methodology tailored to sensitivity for detection for each individual fault has been shown. Hence the test set size is proportional to the number of tested faults which is undesirable. In this section, a collapse algorithm based on the properties of tests optimized for sensitivity to fault detection will be presented.

4.1 Test set collapse algorithm

Given a test configuration, the sensitivity for the detection of a specific fault varies over the parameter space. As illustrated in figures 3 and 4, an increasing area around the optimal parameter value(s) can be identified detecting the modeled fault when increasing its impact. This area will closely correspond to the area enclosed by some tps level value larger than the minimum, if the fault-impact is in the soft-fault tps region The proposed compaction algorithm seeks to **c**ollapse fault-specific best tests $T_{tc,f1}..T_{tc,fn}$ for faults $f_1 \ldots f_n$ into a single test $T_{tc,c}$, if the tests can be grouped in the parameter space. Several groups may be located in the parameter space of the test configuration tc. The test parameter set values in $T_{tc,c}$ are determined by the average of the parameters of the group-members. The collapsing is screened by an evaluation of the cost functions $S_f(T_{tc,f})$ and $S_f(T_{tc,c})$ for the n fault models involved. A parameter δ is introduced which controls the acceptable level of loss in sensitivity due to collapsing. δ denotes the maximal allowed percentile shift of S_f at $T_{tc,c}$ upwards to the level of insensitivity due to collapsing. Insensitivity has cost value '1'. For any fault f_j in the group of faults $f_1..f_n$, the following equation must hold for acceptance of the collapse proposal:

$$S_{f_j}(T_{tc,c}) \leq S_{f_j}(T_{tc,f_j}) + \delta \cdot (1 - S_{f_j}(T_{tc,f_j}))$$

4.2 Results

For the identification of groups, the optimized parameter values of all resulted tests are shown in figure 8 for the test configurations #1, #2 and #3. Since only two tests are defined by test configuration #5, they are shown in Table 3. In figure 8, results which were located

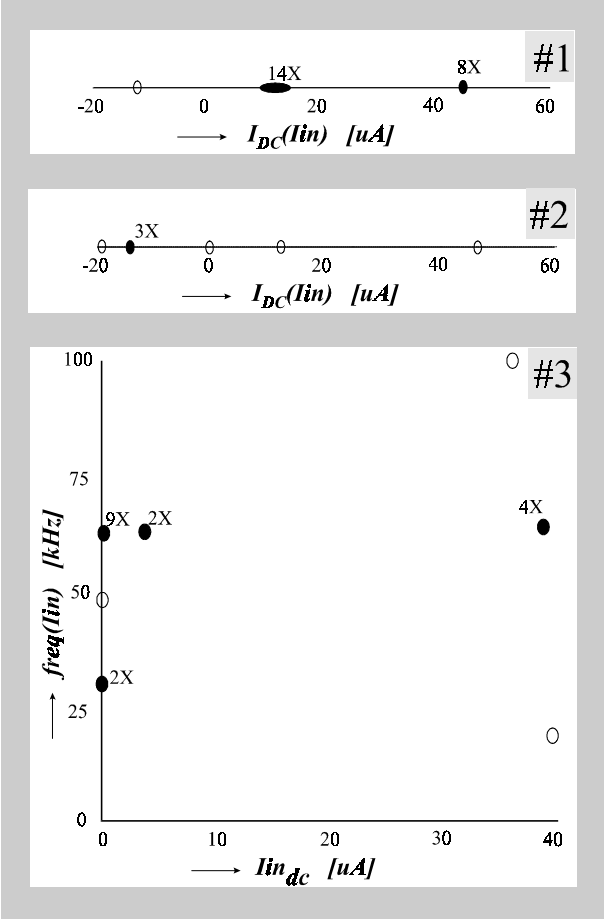

Figure 8: Optimal test parameter values resulting from test configurations #1, #2 and #3.

very close to each other have been considered as candidates for grouping. Groups which have been evaluated for collapsing purposes, are combined in the solid ellipse-shaped areas. An index number denotes the number of tests located in these areas. Empty ellipses surround locations of single test parameter sets. Using a δ

#	par1=base[μA]	par2=elev[μA]
1	1.47	2.26
2	1.49	2.25

Table 3: The optimal solutions which were defined by test configuration #5

of 2%, collapsing of nearly all combined tests would be allowed. The only exception was the group around $T_{\#3}=[Iin_{dc}, freq(Iin)]^T = [39\mu A, 64kHz]^T$ in test configuration #3. This group of 4 tests had to be split into two groups of 2 collapsed tests to satisfy the required δ level. The results shown in table 3 may also be combined. Thus, without really indulging on the obtained sensitivity, a collapsed set of 17 individual tests is obtained. Starting from the original set of 52 tests, this means a compression to 33% of the original size is achieved.

5 Conclusions

A structural, fault-model based methodology for the generation of compact high-quality test sets for analog macros has been presented. Parameters of test configurations have been optimized to sensitivity for detection of each fault in a fault list. Investigation of the distribution along test configuration parameter-axes has been used in a second step to provide a collapsed high-quality test set.

References

[1] M. Sachdev and B. Atzema, "Industrial Relevance of Analog IFA: A Fact or a Fiction", Proc. IEEE International Test Conference 1995, pp. 61-70.

[2] R.J.A. Harvey ea., "Analogue Fault Simulation Based on Layout Dependent Fault Models", Proc. IEEE International Test Conference 1994, pp. 641-649.

[3] N. Nagi and J.A. Abraham, "Hierarchical Fault Modeling for Linear Analog Circuits", pp.89-99 in "Analog Integrated Circuits and Signal Processing", Boston, 1996, Kluwer Academic Publishers.

[4] L. Milor and V. Visvanathan, "Detection of Catastrophic Faults in Analog Integrated Circuits", Proc. IEEE Transactions on Computer Aided Design, vol. 8, no. 2, Februari 1989, pp. 114-130.

[5] M. Sachdev, "A Defect Oriented Testability Methodology for Analog Circuits", Journal of Electronic Testing: Theory and Applications, vol. 6, no. 3, June 1995, pp. 265-276.

[6] V. Kaal and H.G. Kerkhoff, "On the Optimization and Optimal Selection of Tests for Analog/Mixed-Signal Macros", Proc. IEEE International Mixed Signal Testing Workshop 1996, pp. 31-34.

[7] R.P. Brent, Chapter 7 in "Algorithms for Minimization without derivatives", Englewood Cliffs, Prentice-Hall, 1973.

[8] F.S. Acton, pp. 264-267 in "Numerical Methods that Work", Washington, Mathematical Association of America, 1990 corrected edition.

[9] A. Kimmels, "Design of an Integrated Photo Detector for a Laser Doppler Blood Flow Meter", MESA Research Institute report, Enschede, 1995.

[10] K.R. Eckersall ea., "Testing Mixed Signal ASICs Through Use of Supply Current Monitoring", Proc. IEEE European Test Conference 1993, pp. 385-391.