Improved Diagnosis of Realistic Interconnect Shorts

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Abstract

Original diagnostic schemes for wire interconnect shorts are proposed. The idea is to use layout extracted realistic shorts and a broader range of short behaviour assumptions to derive the schemes. Results on real examples clearly show the superiority of the new schemes, both in terms of test size and diagnostic resolution.

1 Introduction

Wire interconnect shorts are a dominant fault type in several kinds of electronic components, from integrated circuits (ICs) and multi chip modules (MCMs) to printed circuit boards (PCBs). Due to the existence of techniques such as boundary-scan these faults can be tested and diagnosed under full controllability / observability conditions for MCMs and PCBs.

There is a variety of schemes for generating diagnostic test sets under these conditions. These schemes fall in two basic categories: the *behavioural* schemes [1, 2, 3, 4, 5, 6, 7] and the less known *structural* schemes that were suggested in [7, 8, 9]. A behavioural scheme produces a test set obtained under the assumption that shorts can be formed by any combinations of nets, regardless of their placement in the layout. A structural scheme produces a test set obtained taking into account only the faulty situations which are physically likely.

The suggestion of structural schemes came about as a means of further reducing the size of test sets. However, since reducing the test set size has not been a major priority in this area, and due to the additional complication of layout dependent tests, this issue has received less attention lately. Nevertheless, with the ever growing complexity of electronic assemblies, test set size is always an issue. Besides, the physical information that the structural methods need can be used not only to reduce the size of test sets but also to reduce diagnostic ambiguity, improving on the time to isolate and repair faults. In fact, having the set of potential realistic faults, the location of a diagnosed fault can be automatically displayed on the layout, drastically improving the task of finding the fault. This physical information can be used with the traditional schemes, to improve diagnostic resolution, without abandoning layout independency.

In this paper, a new family of structural diagnostic methods is proposed. Also, an implementation of the family of structural methods suggested in [7] is presented. The new methods solve some limitations concerning the *diagnostic resolution* of the previously suggested methods.

The paper is organised in the following manner. In section 2 the theoretical background is presented. In section 3 the previous interconnect diagnostic schemes are briefly described. The new diagnostic schemes are proposed in section 4. A statistical method for assessing diagnostic resolution is explained in section 5. Results on real PCB examples are shown in section 6. Finally, in section 7 conclusions and directions for future work are given.

2 Fundamental concepts

In the traditional behavioural schemes, each net n_i of a circuit having N nets is assigned a serial test vector $STV(n_i)$ of length p. Each net responds with a serial response vector $SRV(n_i)$, which is analysed for diagnosis.

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Any short involving multiple nets can be given in terms of a set of basic 2-net shorts. If a 2-net short between nets n_i and n_j is physically possible, we say nets n_i and n_j are neighbours. The information on realistic shorts can be provided by a graph G = (V, E), where each vertex $V_i \in V$ represents a net n_i , and each edge $E_{ij} \in E$ represents a physically possible 2net short between nets n_i and n_j [8]. In this work we used a tool for extracting graph G from a PCB layout, previously presented in [10].

The *edge-distance* between two vertices in a graph is the number of edges on the shortest edge path between the two vertices. The *extent* of a graph is the maximum edge-distance in the graph.

A graph is said to be k-colourable if k colours can be used to colour each vertex in the graph, so that any neighbour vertices are assigned different colours. The set of nets corresponding to the vertices coloured with the same colour is called a *supernet*. Hence, there are k supernets in a circuit whose graph G is k-colourable.

In the previously suggested structural schemes [7] graph G has to be derived and coloured. Although graph colouring is an NP-complete problem, the graphs we have to deal with can be coloured with a few number of colours $(k \ll N)$ using an algorithm described in [8], that was used in this work. This stems from the fact that graphs obtained from PCB layouts are nearly planar. Next, instead of assigning a unique test vector to each net one just needs to assign a unique test vector $STV(s_i)$ to each supernet s_i . In this way much more compact test sets are obtained.

A short is a pair $S = (G_S, f_S)$, where $G_S = (V_S, E_S)$ is a connected subgraph of G defined by the set of shorted nets V_S and by the set of occurring 2-net shorts E_S , and f_S is the short behaviour function. The short behaviour function is usually considered to be a wired-and or a wired-or function. We also consider the strong-driver behaviour, which causes $SRV(n_i) = STV(n_j)$ for any nets $n_i \in V_S$. Net $n_j \in V_S$ is called the strong-driver net.

A stain is a pair $T = (G_T, SRV(T))$, where $G_T = (V_T, E_T)$ is a connected subgraph of G, such that $(V_T, E_T) = (\{n_i \in V : SRV(n_i) = SRV(T)\}, \{E_{ij} \in E : n_i, n_j \in V_T\}).$

To illustrate the concepts above we chose a simple example of a 2-colourable graph, shown in Figure 1. Each net n_i , assigned with $STV(n_i) = 01$ (10), has at most three neighbours n_j assigned with $STV(n_j) = 10$ (01). In the figure one can also see stains T_1 to T_4 , which result from shorts S_1 to S_5 .

Wired-or shorts S_1 and S_2 cause stain T_1 . Had the middle edge in G_{T_1} occurred, forming a single 4-net



Figure 1: Shorts and stains

short, one would not be able to distinguish that situation from the situation presented. This ambiguity is called the *confounding* problem. Stain T_2 is caused by wired-and short S_3 . Similarly to the previous case, confounding happens since the middle edge need not occur in G_{T_2} for stain T_2 to be caused. Stain T_3 is caused by strong-driver short S_4 , where the strongdriver net is one of the peripheral nets. Had the edges connecting only driven nets not occurred, stain T_3 would still happen, and hence it is not possible to decide about the involvement of the driven peripheral nets in S_4 . This ambiguity is called the *aliasing* problem. Stain T_4 is caused by short S_5 and the right most net is aliased as discussed for stain T_3 . The extent of graphs G_{T_1} and G_{T_2} is 3 and the extent of graphs G_{T_3} and G_{T_4} is 2.

Aliasing and confounding were first reported in [5]. However, in practice, the aliasing problem is the important one; the confounding problem is to unlikely to constitute a limitation.

3 The existing diagnostic schemes

The most basic behavioural scheme, called the *counting sequence* scheme, consists of making each test vector equal to the binary numbers 0, 1, 2, ..., N - 1, represented with as many bits as needed to represent N - 1. In this way one obtains the shortest possible set of unique test vectors. Hence the number of bits p needed for each test vector is given by

$$p = \lceil \log_2 N \rceil. \tag{1}$$

Assigning the counting sequence scheme to the supernets, one obtains the previously suggested structural counterpart of the behavioural counting sequence test set. In Figure 2 a 3-colourable graph is shown, for which the structural counting sequence test set is given in Table 1.



Figure 2: A 3-colourable graph G

Supernets	Nets	MTV	
<i>s</i> ₁	n_2	0 0	
s_2	n_1, n_4, n_5	0 1	
s_3	n_3	10	

Table 1: Counting sequence test set for graph G of Figure 2

The behavioural counting sequence scheme guarantees detection of any shorts S for, according to the assumed short behaviours, $SRV_j \neq STV_j$ for at least one net $n_j \in V_S$. Observing that only neighbour nets can short, the same result holds for the structural counting sequence method, while using test vectors having only $\lceil \log_2 k \rceil$ bits, according to equation (1).

However, the diagnostic capabilities of the counting sequence schemes, both behavioural and structural, are poor due to the aliasing problem mentioned in section 2. To avoid this problem, the well known counting sequence plus complement scheme [3] can be used. This test set is formed by concatenating each counting sequence vector with its complement, producing twice as long test vectors. As it can be demonstrated, the behavioural counting sequence plus complement test set is aliasing free for all the three short behaviours considered. However, the structural counterpart of this method is aliasing free for all but the strong-driver short behaviour. As a matter of fact, with such a scheme, strong-driver aliasing as shown in section 2 for stains T_3 and T_4 can still happen.

4 The new diagnostic schemes

To completely get rid of aliasing in the previously suggested structural schemes one should observe the following: the properties of the behavioural test sets are inherited by their structural counterparts as long as stains involving nets assigned with the same serial test vector do not happen.

In practice, the occurrence probability of faulty situations causing stains whose graphs have an extent greater than a value ε can be neglected. Thus, the desired diagnostic capabilities need apply only for stains whose extents are lower than ε . The value ε can be set according to the needed diagnostic capability.

Bearing this in mind, we propose a family of enhanced structural test sets obtained as follows. A graph G_{ε} is constructed, which has the same vertices and edges as G plus extra edges between every pair of vertices whose edge-distance is ε or lower. An algorithm for deriving G_{ε} from G having time complexity $O(\varepsilon \times N^3)$ is used. In Figure 3, we show graph G_2 obtained from graph G of Figure 2. The extra edges are shown in dashed lines. The next step is to k-colour graph G_{ε} . After this step any nets in any subgraph of G with extent ε or lower are assigned different colours. Applying the graph colouring procedure to graph G_2 in Figure 3 yields the 4-colour mapping shown in the same figure. The last step of our method, similarly to the previously suggested structural methods, is to assign a behavioural test set to the supernets thus obtained.



Figure 3: The 4-colourable graph G_2 derived from graph G of Figure 2

It should be said that the triangulation transformation presented in [11] is equivalent to constructing graph G_2 in our approach. However, in that paper it was not recognised that for stains with extents greater than 2 full diagnostic capability cannot be claimed.

5 Assessing diagnostic resolution

To be able compare the new diagnostic schemes with the existing ones we developed a *statistical diagnostic simulator*. The algorithm of the simulator is rather complex and will not be described in detail since it is not the main thrust of this paper.

It will suffice to say that the simulator works by generating r-edge shorts up to a multiplicity r_{max} , and computing the average *diagnosability* d_j^r of each r-edge short S_j^r by

$$d_j^r = E(\frac{r}{\#E_{T(S_j^r)}}),\tag{2}$$

where $T(S_j^r)$ is the stain caused by short S_j^r and E()stands for the average over all short behaviours. That is, d_j^r is the average ratio of the number of edges in S_j^r by the number of candidate edges in $E_{T(S_j^r)}$. Hence, the overall diagnostic resolution DR is given by

$$DR = \sum_{r=1}^{r_{max}} \sum_{j=1}^{U^r} d_j^r P(S_j^r),$$
(3)

where U^r is the number of *r*-edge shorts simulated and $P(S_j^r)$ is the relative occurrence probability of short S_j^r . The values U^r have to be large enough to assure statistical convergence of DR. The values $P(S_j^r)$ are obtained using the well known generalised negative binomial statistics, which has been shown to apply to PCB faults [12]. Note that, as a consequence of equation (2), $0 < d_i^r$, $DR \leq 1$.

6 Results

A set of real PCB layouts whose characteristics are outlined in Table 2 was used.

Board	#Cmps	#Nets	#Pins
ir232	24	22	80
68hc11	54	93	332
sram8	47	120	680
cperi24	79	271	952

Cmps = components

Table 2: Board examples

In Table 3, the test set lengths for the various schemes are shown. The test sets determined are the counting sequence test set CS and the counting sequence plus complement test set CC. Subscripts b, s and e are used with CS and CC to identify the three cases: behavioural test sets (b), previously suggested structural test sets (s) and enhanced structural test sets (e). The enhanced structural test sets were obtained with $\varepsilon = 2$.

Board	CS_b	CC_b	CS_s	CC_s	CS_e	CC_e
ir232	5	10	3	4	4	6
68hc11	7	14	3	6	6	10
sram8	7	14	3	6	5	10
cperi24	9	18	3	6	7	14

Table 3: Test vector length results

As one can see, the new enhanced structural schemes do not produce as short a test set as the previously suggested structural schemes, but still produce significantly shorter test sets than the traditional behavioural schemes. The reason for this is their improved diagnostic resolution, as will be shown.

In Table 4 the diagnostic resolution results are shown. For the diagnostic simulations, the values $r_{max} = 6$ and U(r) = 1000 were used. In the behavioural schemes CS_b and CC_b , a fully connected graph G was used to count the number of candidate edges $E_{T(S_j^r)}$ (see equation (2)), since the assumption inherent to these methods is that any 2-net shorts are candidate shorts.

Board	CS_b	CC_b	CS_s	CC_s	CS_e	CC_e
ir232	.839	.916	.604	.881	.915	.981
68hc11	.789	.921	.592	.798	.862	.988
sram8	.824	.919	.556	.838	.881	.997
cperi24	.802	.919	.466	.709	.854	.995

Table 4: Diagnostic resolution results

Analysing this table, one notices that, in general, the test sets CC perform much better than the test sets CS, which shows agreement of our simulations to this empirical fact. Comparing the behavioural schemes to the previously suggested structural schemes, one can see that the latter achieve lower diagnostic resolution than the former. This fact makes the previously suggested structural schemes less interesting, in spite of the their producing a shorter test set. However, the new enhanced structural schemes have excellent diagnostic resolution, the best when compared to the previous two families. This justifies their extra test set length when compared to the previously suggested structural tests.

It could also be shown that if structural information (graph G) is used with the behavioural test sets in diagnosis, similarly high diagnostic resolution can be achieved. This provides a means to improve diagnostic quality without giving up layout independent test sets.

Finally, we discuss the computational time involved in structural diagnosis. $O(N^3)$ algorithms were used to produce the structural test sets. For large examples, of a few tens of thousands of nets, we estimate these algorithms are inadequate. Nonetheless, as we could show, the algorithms can be optimised to $O(N^2)$. These would take a few hours on the large examples, which is an acceptable time for test preparation.

7 Conclusion

The traditional behavioural schemes for interconnect shorts diagnosis have the desirable features of being layout independent and producing an acceptable test vector length in most practical cases. However, giving up layout independence they can be further improved in terms of length. They can also be used as they are in conjunction with structural diagnostic information, to produce outstanding diagnostic resolution.

The family of structural schemes suggested in [7] was implemented. These schemes produce shorter test sets than the behavioural schemes but their diagnostic resolution is lower than the diagnostic resolution of the traditional schemes. This has to do with their weak diagnosis of strong-driver shorts.

An enhanced version of structural schemes was proposed. These methods produce longer test vectors than the previously suggested structural schemes, but still significantly shorter test vectors than the behavioural schemes. However, their diagnostic resolution is the best when compared to the other two families of methods.

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References

- William H. Kautz. "Testing for Faults in Wiring Networks". *IEEE Transactions on Computers*, C-23(4):358-353, April 1974.
- [2] P. Goel and M.T. McMahon. "Electronic Chip in Place Test". In Proc. Int. Test Conference (ITC), pages 83-90, 1982.
- [3] P.T. Wagner. "Interconect Testing with Boundary Scan". In Proc. Int. Test Conference (ITC), pages 52-57, 1987.
- [4] A. Hassan, J.Rajski, and V.K. Agarwal. "Testing and Diagnosis of Interconnects using Boundary Scan Architecture". In Proc. Int. Test Conference (ITC), pages 126-137, 1988.
- [5] N. Jarwala and C.W. Yau. "A New Framework for Analyzing Test Generation and Diagnosis Algorithms for Wiring Interconnects". In Proc. Int. Test Conference (ITC), pages 63-70, 1989.
- [6] C.W. Yau and N. Jarwala. "A Unified Theory for Designing Optimal Test Generation and Diagnosis Algorithms for Board Interconnects". In Proc. Int. Test Conference (ITC), pages 71-77, 1989.
- [7] WT Cheng, J.L. Lewandowski, and E. Wu. "Diagnosis for Wiring Interconnects". In Proc. Int. Test Conference (ITC), pages 565-571, 1990.
- [8] M.R. Garey, D.S. Stifler, and H.C. So. "An Application of Graph Coloring to Printed Circuit Testing". *IEEE Trans. on Circuits and Systems*, CAS-23(10):591-599, Oct. 1976.
- [9] J.L. Lewandowski and V.J. Velasco. "Short Circuit Testing". Technical Report CC8559, AT&T, October 1986.
- [10] J.T. Sousa, T.Shen, and P.Y.K. Cheung. "Realistic Fault Extraction for Boards". In Proc. European Design and Test Conference (ED&TC), 1996.
- [11] D. McBean and W.R. Moore. "Testing Interconnects: A Pin Adjacency Approach". In Proc. European Test Conference (ETC), pages 484-490, 1993.
- [12] Mick M.V. Tegethoff. "Defects, Fault Coverage, Yield and Cost in Board Manufacturing". In Proc. Int. Test Conference (ITC), pages 539-547, 1994.