

PANEL: NOISE AND SIGNAL INTEGRITY IN DEEP SUBMICRON DESIGN

Chair: William E. Guthrie, Collett International, Inc., Santa Clara CA

Organizer: Massoud Pedram, University of Southern California, Los Angeles CA

Abstract

Sub-half-micron process technologies are creating a fundamental shift in the problems faced by IC designers and fabricators. As geometries shrink, signal integrity (SI) and noise play a critical role in determining IC performance. Without accurate interconnect data and detailed noise analysis tools, designers cannot assess the quality of their designs and/or new processes.

This panel will offer designers an opportunity to understand the complex analysis and design issues that surround the noise and signal integrity problem. More precisely, it will seek to answer the following questions.

- 1 What is the source, scope and magnitude of SI/noise problems facing IC/ASIC designers today?
- 2 Under what design conditions and scenarios do serious noise and signal integrity problems occur?
- 3 How important are SI/noise issues relative to interconnect delay, design complexity, verification concerns?
- 4 How have SI/noise problems impacted design cycle times, performance, parametric yield?
- 5 Are practical, mainstream tools/methodologies available today to deal with these issues? If so, are they focused on back-end (layout) or front-end (synthesis) flows?
- 6 Are tools/flows designed to prevent SI/noise problems, or detect and correct them?
- 7 How does the choice of design style (static logic vs. dynamic logic, etc.) affect SI/noise susceptibility?
- 8 What long range changes in design tools and practices do you anticipate?
- 9 Will designers need new skills, or will the design infrastructure (tools, methodologies, libraries) hide the problems?

Embedded Tutorial

Wayne Dai
University of California, Santa Cruz CA

It was projected by the National Technology Roadmap for Semiconductors that by the year 1998 the feature size will shrink to 0.25 μ m and chips may contain as many as 28 million transistors. As the results, interconnect delay on chip dominates the gate delay and delay will not be calculated accurately without taking into account the cross-talk.

This calls for 3D parasitic extraction. However, it is prohibitively expensive to extract every net 3D; in fact, it is not necessary to do so. A multi-tiered extraction methodology is required.

After classifying 2D, quasi-3D, and 3D parasitic extraction, I will present a multi-tiered full chip extraction methodology which consists of lumped-C filtering, 2D RC screening, and 3D critical net extraction. I will next survey 3D critical net extraction in detail. One way is to extract a net, or at least a segment of a net as whole, based on a full 3D field solution or a Monte Carlo integration ("random walk"). Another way is to cut and paste a net with tolerable boundary effect so that most of the 3-D structures can be pre-characterized in a 3D interconnect library. Some current standardization efforts, including SEMATECH Chip Parasitic Extraction and Signal Integrity Verification project, will be presented to facilitate the seamless integration between high capacity 2D extractors from major vendors and high accuracy 3D extractors from niche players.

The tutorial will end by posing a few challenges in signal integrity (simultaneous switching and cross-talk) and signal reliability (electro-migration) which leads to the panel discussion which immediately follows the tutorial. For more details, please refer to the companion paper entitled "Chip Parasitic Extraction and Signal Integrity Verification" in this Proceedings.

Position Statements

Rakesh Chadha
Bell Laboratories, Murray Hill NJ

The signal integrity noise problems have become critical and can no longer be ignored for deep submicron designs. These problems are caused by various forms of crosstalk coupling in the chip - power and ground coupling, substrate coupling and crosstalk between neighboring nets. These couplings may cause a minor glitch, affect the timing and in some cases alter the intended functionality of the design.

The design methodologies in use today require the designers to select portions of the design for potential problems and verify whether a problem exists through detailed device level simulations for these portions. The dynamic and full custom designs are especially susceptible to the signal integrity noise problems. The designers are aware of these problems and are thus conservative in pushing the technology limits. These problems have also increased the cycle time and number of iterations.

The designers need automated and efficient tools to point to areas of designs where potential problems exist. The related need is for efficient tools to flag the violations. The designers would then use their skills and correct and fix only those cases where the problem exists and can then stretch the technology limits.

Jason Cong
University of California, Los Angeles CA

Due to the rapid scaling of IC technology, decrease of supply and threshold voltage, and the increase of circuit speed, noise is no longer a problem associated with a few 'special nets', but a serious concern with many signals. It is no longer feasible to go through a lengthy iteration of design, simulation, re-design, and re-simulation to fix the noise problem for a few nets after circuit and layout design. Yet imposing a set of overly conservative design rules for all signals often results in high penalty on circuit area and performance. It is necessary to develop efficient physical design algorithms and tools to control the noise and maintain signal integrity during the layout design process, with the same emphasis as area, delay, and power optimization. This requires first developing accurate yet efficient noise models to be incorporated into the layout tools. Based on these model, existing layout optimization techniques for delay minimization, such as routing topology optimization, buffer insertion, device and interconnect sizing, shall be extended to address the noise and signal integrity issues. New techniques, such as variable wire spacing, wire ordering and shielding, and multi-layer assignment, shall also be incorporated into the automatic layout systems for noise control and minimization.

Charlie Xiaoli Huang
Synopsys Inc., Mountain View CA

Signal integrity and noise issues will force another significant overhaul to design style, design methodology, and design tools, just as the so called interconnect delay crisis did during the past few years. Unfortunately, solutions to these issues may prove to be more elusive than those for dealing with interconnect delay.

Many factors often have to be considered simultaneously and evaluated carefully to uncover potential noise problems. Global or local power supply variations may lead to reduced noise margins and false switching. They may also cause variations in gate delays that lead to timing errors. A glitch introduced through cross-coupling capacitance may directly lead to functional failures in latches or dynamic logic circuits. Cross-coupling capacitance, a significant portion of total wire capacitance, can also give rise to significant changes in wire delays, which is already the dominant delay for many signal nets.

These problems defy conventional static or dynamic analysis. In static analysis, a limited signals are considered active, whereas analysis of cross coupling effects and power fluctuation requires consideration of activities of multiple signals. For dynamic analysis to expose such problems,

vectors must be selected to trigger simultaneous signal switching as well as cover the possibility of the relative timings of these simultaneous switching, which makes this approach prohibitively time consuming. New tools employing new techniques will have to be developed to address these problems.

In addition to analysis tools, design style and practice will need to be reassessed. The merits of pass transistor logic, dynamic logic, differential logic, and even synchronous logic, will have to be reassessed.

Anirudh Devgan
IBM Austin Research Laboratory, Austin TX

Deep submicron issues, such as noise and signal integrity, invariably make design methodologies more complex. This complexity in design methodology has be weighed with other circuit design and process technology options in selection of a design point. High performance designs mandate minimizing the analysis uncertainty. Detailed noise and signal integrity analysis techniques are critical to insure correct circuit operation and to achieve maximum performance. Furthermore, back-end analysis has to be strongly complemented by signal integrity and noise avoidance techniques during logic, circuit and physical design.

Tom Mozdzen
Intel, Chandler AZ

The importance of signal integrity for long signal lines is on par with the delay. On-chip inductance will mainly affect power lines and the clock, and can be handled separately. Scaling trends are increasing cross-talk and cross capacitance factors on signal lines to the point where the minimum metal pitch is unusable on long lines. A line may be susceptible to cross-talk when a section of the line near the receiver is heavily coupled to other lines and is isolated from its driver either from RC or transmission line effects. Cross-talk intelligent routing and extraction tools are needed to avoid the present day fixes of blindly raising the metal pitch on all lines, inserting repeaters, or tediously checking each offending line for real violations.

Andrew Yang
Avant! Corp., Sunnyvale CA

Signal integrity problems include capacitive coupling, di/dt signal bounce, substrate noise, and clock skew. In addition, power integrity problems such as IR drop can also lead to serious timing failure in high-performance CPU and ASICs. Current verification tools are addressing full-chip parasitic extraction including network reduction and subsequent simulation and analyses. The challenge is to handle complex designs over 10 million transistors while taking into account more and more physical information important to signal and power integrity analyses. Next generation signal verification tools will need to migrate up-stream for tighter integration with physical designs and timing estimation tools.