Advances in IC process technology have enabled the design of complex systems on a single chip. System-on-chip developers need to be able to mix and match pre-designed, best-in-class functional blocks from many providers if they are to meet design deadlines with limited design engineering resources. Consequently, there is a rising interest in the creation, distribution, and design application of reusable, interoperable blocks of intellectual property, referred to as "IP" or "virtual components." This panel will explore the opportunities and challenges for design innovation offered by a worldwide, open reuse mechanism for virtual components.

The session will begin with an embedded tutorial case study on the VSIA (Virtual Socket Interface Alliance) approach to design reuse. Then IP providers and users will discuss the technical and business challenges in establishing a mechanism for reuse of virtual components. The panelists will also discuss the issues in integrating virtual components from multiple providers into system-on-chip designs.

Doug Fairbairn, Cadence Design Systems
Larry Cooke, Toshiba America Electronic Components

The VSI Alliance was formed to help drive a common vision for the use of complex cores in the electronics industry and break down the technical barriers to the mix and match of IP in system-on-chip design, including new concepts such as "virtual components" and the "virtual socket interface." This tutorial will describe the background of the VSI Alliance, including the industry forces which brought it into existence. We will present the first results of the Alliance, including the VSI Architectural Document and Roadmap and how these can be applied to system-on-chip design. We will also provide a brief review and description of potential impact of the Alliance's work in progress in areas such as IP protection, mixed-signal design, manufacturing test, system-level design, implementation/verification, and on-chip bus standards.

Steve Schulz, Texas Instruments

After evaluation, virtual components will be designed into the system-chips of the future using new methodologies. This presentation will cover how virtual components are captured, starting from an English requirements definition through the conversion to netlists, including hardware/software, board, ASIC, and FPGA technologies. It will also describe how virtual components are captured when netlists are converted to real physical instantiations. There will be descriptions of the documentation, formats, and design interfaces required to facilitate "plug-and-play" productivity gains, as well as realistic views of required application support for various types of virtual components.

Takahide Inoue, Sony

Probably the most profitable and often-used virtual components in system houses are standard formats such as NTSC, Ethernet, and PCI bus. The emerging System-on-Chip (SoC) integration capabilities require system industries and semiconductor manufacturers to develop strong technical and business collaborations, since now more than ever, SoCs must be designed with reliable semiconductor technology.

Another challenging subject in the industry is the need for the management of reusable virtual components. A "meet-on-silicon" methodology with large pre-designed, sub-system virtual components is a viable direction in terms of design efficiency and product management. However, it needs vigorous development by design tool suppliers, which must integrate technology for the search and evaluation, system modeling, and verification of virtual components within a robust hardware/software co-design environment.

Raj Raghavan, Virtual Chips

This presentation will describe electronic commerce and details of business transactions of the future for dealing with virtual components. It will include details of the different types of transactions, such as low-support vs. support-intensive; customized, license-only versus license-plus-royalty, etc. It will also describe models for negotiating and quickly concluding appropriate agreements, and models for tracking IP usage and royalty payments.

Jean-Louis Bories, LSI Logic

The various aspects of system-on-a-chip design include processes, methodologies, tools, and IP. All of these aspects are needed in order to fill the gap between process technology and design capability. In this context, interface standards to make IP reusable, scaleable, and fit into the ASIC environment become a necessity. Without standards, the reuse of various categories of IP (varying by complexity and performance) can only be achieved within a resource-intensive environment. This contradicts the time-to-market and right-first-time requirements of system-on-a-chip design.

Wally Rhines, Mentor Graphics

Thousands of innovative designers need a vehicle for capturing their ideas in silicon. The biggest barriers to IP-based
innovation are support and verification: how can users maintain the most up-to-date and highest-quality intellectual property? How can they target specific processes and foundries? And how can they verify that all the virtual components work together at the system level?

EDA suppliers must continue to play their traditional role in supporting system designers with best-in-class tools, flows, and virtual components. However, they must now redouble their efforts by supporting virtual components in real design flows and making them truly reusable. EDA companies that adopt an "IP publisher" model are best-positioned to meet the challenges associated with worldwide design reuse by providing widespread access to tool independence, virtual components, and knowledge-sourced targeting and customization.
Session 24 Participants
Panel: Challenges in Worldwide IP Reuse
Embedded Tutorial: Applying VSIA Standards to System Chip Design

Jean-Louis Bories
VP and General Manager of ASIC Technology
LSI Logic Corporation
1525 McCarthy Blvd., MS E-188
Milpitas, CA 95035
Tel: 408-433-6722
Fax: 408-433-7811
Email: jlouis@lsil.com

Laurence H. Cooke
Chief Technologist, SID Engineering
Toshiba America Electronic Components, Inc.
1060 Rincon Circle
San Jose, CA 95131
Tel: 408-526-2860
Fax: 408-456-9286
Email: larry.cooke@taec.com

Doug Fairbairn
President, Virtual Socket Interface Alliance
VP, Cadence Design Systems, Inc.
2655 Seely Ave.
San Jose, CA 95134
Tel: 408-428-5767
Fax: 408-944-7168
Email: doug@cadence.com

Rita Glover
President & Principal Analyst
EDA Today, L.C.
10645 N. Tatum, Suite 200-609
Phoenix, Arizona 85028
Tel: 602-443-9209
Fax: 602-443-9211
Email: ritag@edat.com

Takahide Inoue
VP & Senior Technology Advisor
Sony Corporation of America
530 Cottonwood Drive
Milpitas, CA 95035
Tel: 408-955-4279
Fax: 408-955-6070
Email: inoue@itc.sca.sony.com

Raj Raghavan
VP, Virtual Chip Products
Phoenix Technologies Ltd.
411 E. Plumeria Drive
San Jose, CA 95134
Tel: 408-570-1000
Fax: 408-570-1001
Email: raj@vchips.com

Laurence H. Cooke
Chief Technologist, SID Engineering
Toshiba America Electronic Components, Inc.
1060 Rincon Circle
San Jose, CA 95131
Tel: 408-526-2860
Fax: 408-456-9286
Email: larry.cooke@taec.com

Doug Fairbairn
President, Virtual Socket Interface Alliance
VP, Cadence Design Systems, Inc.
2655 Seely Ave.
San Jose, CA 95134
Tel: 408-428-5767
Fax: 408-944-7168
Email: doug@cadence.com

Rita Glover
President & Principal Analyst
EDA Today, L.C.
10645 N. Tatum, Suite 200-609
Phoenix, Arizona 85028
Tel: 602-443-9209
Fax: 602-443-9211
Email: ritag@edat.com

Takahide Inoue
VP & Senior Technology Advisor
Sony Corporation of America
530 Cottonwood Drive
Milpitas, CA 95035
Tel: 408-955-4279
Fax: 408-955-6070
Email: inoue@itc.sca.sony.com

Raj Raghavan
VP, Virtual Chip Products
Phoenix Technologies Ltd.
411 E. Plumeria Drive
San Jose, CA 95134
Tel: 408-570-1000
Fax: 408-570-1001
Email: raj@vchips.com

Walden C. Rhines
President & CEO
Mentor Graphics Corporation
8005 S.W. Boeckman Road
Wilsonville, Oregon 97070-7777
Tel: 503-685-1006
Fax: 503-685-6972
Email: wally_rhines@mentorg.com

Steven E. Schulz
Senior Member, Technical Staff
EDA Systems, Semiconductor Group
Texas Instruments Inc.
7839 Churchill Way, MS 3937
Dallas, TX 75251
Tel: 972-917-3648
Fax: 972-917-7966
Email: ses@dad.ti.com

John Teets
Program Manager, EDA Industry Council
Technology Program Manager, CAD Framework Initiative
4030 West Braker Lane, Suite 550
Austin, Texas 78759
Tel: 512-342-2244 x 57
Fax: 512-342-2037
Email: teets@cfi.org