# Statistical Estimation of Average Power Dissipation in Sequential Circuits *

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## Abstract

In this paper, we present a new statistical technique for estimating average power dissipation in sequential circuits. Due to the feedback mechanism, in sequential circuits power dissipation in consecutive clock cycles are temporally correlated, which violates the basic requirement of statistical mean inference procedures. We overcome this problem by using a randomness test and a sequential procedure to select a proper independence interval, which in turn is used to generate random power samples. A distribution-independent stopping criterion is applied to analyze the sample data and terminate the simulation upon achievement of the accuracy specification. The technique is successfully applied to a set of benchmark circuits.

## I. Introduction

Accurate power analysis poses a great challenge to both VLSI circuit designers and design automation engineers. For designers, evaluation of battery life in portable equipment and assessment of several reliability problems rely on accurate power analysis. For design automation engineers, accurate and fast power analysis is essential to developing efficient CAD tools for power optimization. Thus, power estimation has become the focus of research efforts in recent years.

Depending on the abstraction level, circuit entity for which power dissipation needs to be analyzed varies. At gate level, combinational and sequential circuits are the objects of power estimation. For combinational circuits, average power can be estimated by a probabilistic or statistical technique which propagates switching activity statistics at the primary input terminals through the circuit and monitors the power dissipation. Due to the feedback mechanism, power estimation in sequential circuits is, however, much more complicated. A sequential circuit contains both primary inputs and latch inputs. While the switching characteristics of primary inputs are determined by the operating environment, those of latch inputs also depend on the implemented finite-state machine (FSM), which causes spatial and temporal correlations among latch input signals. Considering these effects in power estimation greatly increases the complexity of the problem.

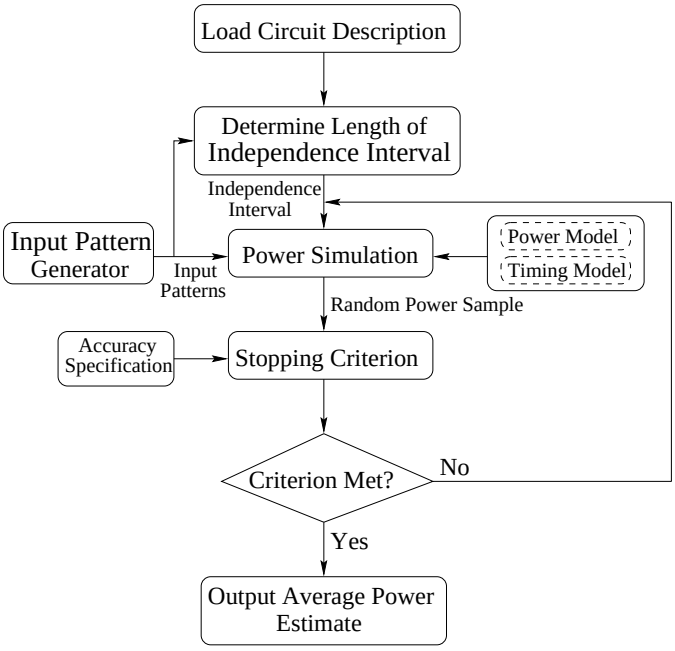


Figure 1: Flowchart of the proposed power estimation approach.

To tackle this problem, most of the existing approaches choose to partition a sequential circuit into its combinational part and the latches and then analyze their contribution separately. The statistical characteristics of the FSM is first lumped into the switching activity metrics (signal probabilities and transition densities) of the latch inputs by either a long-time logic simulation [1] or solving a set of nonlinear equations [2, 3, 4]. Power dissipation of the combinational part can then be analyzed as mentioned above using such information. A major drawback of these approaches is that spatial and temporal correlations among latch signals are not considered. As the average power is very sensitive to signal correlations [5], neglecting such information will yield poor estimation accuracy.

To overcome this drawback, we propose a new statisti-

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cal approach, as depicted in Fig. 1. This approach takes full account of signal correlations among latches as well as internal nodes. Statistical techniques require a random sample, i.e., a sample of *independent and identically distributed*(iid) power data, for mean estimation. In sequential circuits, however, power dissipations in consecutive clock cycles are temporally correlated. To handle this problem, we propose to use a *randomness test* to determine a proper *independence interval* over which the circuit should be simulated between two power sampling cycles. Randomness test examines the validity of the hypothesis that a power sequence is composed of iid's by *accepting* or *rejecting* the hypothesis according the statistical evidence gathered from the sequence. At a trial independence interval, if the hypothesis is accepted with a user-specified *significance level*, the sequence can be viewed as a random sample. Otherwise, the trial interval is incremented and another power sequence is collected. The iteration continues until the hypothesis is accepted and the associated independence interval is used hereafter to generate random power samples. A distribution-independent stopping criterion is then used to continuously analyze the power sample data and control the sample size until the desired accuracy is achieved. In addition to high estimation accuracy by considering all signal correlations, the simulation efficiency is also greatly improved by the dynamic selection mechanism of the independence interval.

The rest of the paper is organized as follows. In Section II we formulate the average power dissipation problem as a mean estimation problem by expressing power as a random quantity. The difficulties of mean estimation in sequential circuits are also highlighted. In Section III, we first explain how to generate a random sample from a sequential circuit. then we introduce the randomness test as the core of a sequential procedure to determine a proper independence interval. A distribution-independent stopping criterion is selected in Section IV to measure the convergence of the average power estimate. The proposed technique is implemented and tested on a set of benchmark circuits. Section V reports and discusses the experimental results, followed by concluding remarks in Section VI.

## II. Problem Formulation

A sequential circuit is composed of a set of latches and a combinational block. When the latches are triggered, the values present at the latch inputs are captured and transferred to their outputs and fed into the circuit. An *input pattern* is a binary vector received by the primary inputs. The statistics of input patterns vary with the operating environment the circuit is embedded in. Because of its random nature, the input pattern can be treated as a random variable, denoted hereafter as $\boldsymbol{V}$. Along with the input pattern, the *present state vector* of the circuit determines its *next state vector*. The statistics contained in state vectors depend not only on the FSM realized by the circuit but also on the statistics of input patterns. Hence, state vector is also a random quantity denoted as $\boldsymbol{S}$.

Except for very low voltage technologies, logic state transition accounts for the major power-dissipating event in a cell (logic gate or memory element). For a circuit with $N_g$ gates, the power dissipation can be expressed as a function of present input pattern $\boldsymbol{V}_1$, present state vector $\boldsymbol{S}_1$, next input pattern $\boldsymbol{V}_2$, and next state vector $\boldsymbol{S}_2$:

$$\boldsymbol{P} = \frac{V_{DD}^2}{2T} \sum_{i=1}^{N_g} C_i \boldsymbol{n}_i(\boldsymbol{V}_1, \boldsymbol{S}_1, \boldsymbol{V}_2, \boldsymbol{S}_2), \qquad (1)$$

where $C_i$ is the load capacitance at node $i$, $\boldsymbol{n}_i$ is the number of transitions occurred at node $i$, $T$ is the clock cycle time, and $V_{DD}$ is the power supply voltage. Depending on the desired accuracy in the power dissipation model, $C_i$ can be adjusted to take into account additional contributions from short circuit current, internal capacitance charging/discharging, etc.

Since $\boldsymbol{P}$ is a function of random variables $\boldsymbol{n}_i$, $i = 1, \cdots, N_g$, it is also a random variable and possesses a distribution function. Thus, the average power of the circuit can be expressed as the expected value of $\boldsymbol{P}$. Compared to the formulation of combinational circuits [7], however, $\boldsymbol{P}$ is no longer a function of iid's. Because of the feedback, $\boldsymbol{S}_2$ is a function of $\boldsymbol{V}_1$ and $\boldsymbol{S}_1$. Hence $P_1, P_2, \ldots, P_n$, power dissipations of the circuit in $n$ consecutive clock cycles, are temporally correlated. Thus, this sequence should be viewed as a *realization* of a *random process* $\{\boldsymbol{P}_j\}$ from $j = 1$ to $j = n$. Since statistical mean estimation procedures require random samples, $P_1, P_2, \ldots, P_n$ cannot be directly used.

## III. Generation of Random Power Sample

For sequential circuits, a random power sample can be generated either by analyzing the FSM and conduct power simulation accordingly, or by processing the observed power data directly. The first approach works as follows. For sequential circuits, if we know the state transition graph (STG) of the FSM, we can solve the Chapman-Kolmogorov equations for the stationary state probabilities [12]. According to these information, a present state vector can be randomly generated and, along with a present input pattern, determines the next state vector. With a random next input pattern (generated according to the statistics of input streams), power dissipation can be obtained via circuit simulation. In this case, power data are random in nature and compose a random sample. Unfortunately, in real life, a typical sequential circuit usually has a large number of latches. The FSM can easily become too large to be extracted because of its exponential complexity with the latch count. It also takes extra efforts to handle correlations in input streams. Since the state probabilities are jointly determined by the statistics of input patterns and the FSM, computationally it could be prohibitively expensive to solve the Chapman-Kolmogorov equations for these information.

An alternative is to *implicitly* solve the Chapman-Kolmogorov equations using a proper warm-up period. The transition behavior of an FSM is characterized by its *state*

*transition matrix* **P**. For an FSM with $N$ states, **P** is a $N \times N$ matrix with elements $0 \leq p_{ij} \leq 1, i, j = 1, \ldots, N$. $p_{ij}$ is the transition probability from state $S_i$ to $S_j$. **P** is, of course, unknown and is unlikely to be extracted because of the complexity issues. Given an arbitrary initial probability distribution vector **p**(0), after $k$ clock cycles the $k$-step probability distribution vector **p**$(k)$ is

$$\mathbf{p}(k) = \mathbf{p}(0)\mathbf{P}^k. \tag{2}$$

Matrix $\mathbf{P}^k = \overbrace{\mathbf{PP}\ldots\mathbf{P}}^{k \text{ times}}$ is the $k$-step transition matrix. For an ergodic Markov process, as $k$ gets larger, **p**$(k)$ will become increasingly independent of **p**(0) and will approach $\mathbf{p}_s$, the stationary state probability distribution vector. Therefore, with a proper warm-up period $k$, the probability that an arbitrary state is observed will converge to its stationary state probability. However, due to the lack of knowledge on **P**, assumptions need to be made inevitably in order to determine $k$. For example, Chou et al. [9] assumed that an FSM has two nearly-closed sets of states with very small transition probabilities between them. This is a conservative assumption and may lead to a warm-up period much longer than necessary for FSM's with better transition behavior.

The second approach is to "extract" a random sample directly from the observed correlated power sequence instead of starting from the STG. A random sample can be viewed as a sample generated from an iid random process [15]. Thus, our task is equivalent to extracting an iid sequence from the original time series. In order to do this, we assume that $\{\boldsymbol{P}_j\}$ is $\phi$-mixing [16] and stationary with finite variance. Both assumptions have already been made in the first approach. Simply put, $\phi$-mixing refers to the property that the distant future behavior of $\{\boldsymbol{P}_j\}$ becomes increasingly independent of its past as they get further apart in time. Given an observed power sequence $P_1, P_2, \ldots, P_n$ from $\{\boldsymbol{P}_j\}$, by stationarity each $P_k, k = 1, \ldots, n$ has the same distribution function $F(p)$. If there exists an interval of $m$ clock cycles such that $P_k$ and $P_{k+m}$ are independent, then $P_1, P_{1+m}, P_{1+2m}, \ldots$ will be an iid sequence, again by stationarity. By the $\phi$-mixing assumption of $\{\boldsymbol{P}_j\}$, the existence of $m$ is guaranteed. In other words, if we can somehow find $m$, the independence interval, a random sample can be constructed simply by recording the power dissipation in the circuit once for every $m$ clock cycles. In the following, we propose to use a randomness test to examine the statistical independence of the data in a power sequence. Based on the test, we develop a sequential procedure to dynamically choose a proper independence interval, which is then used to generate a random sample.

### A. Hypothesis Test for Randomness

Randomness test [13] belongs to the category of nonparametric hypothesis test which verifies the validity of a statistical hypothesis on the distribution or certain property of a random variable. As the name indicates, randomness test is used to examine the randomness of a data sequence. In this paper, the *ordinary runs test* is adopted among others. The ordinary runs test handles an ordered sequence of data in two symbol types. In one such sequence, a *run* is defined as a succession of one or more identical symbols, which are followed and preceded by the other symbol or no symbol at all. The hypothesis of the test is that the sequence is randomly generated. If the hypothesis is true, the number of runs has a normal distribution. Nonrandomness is reflected in a sequence by either a tendency to cluster the elements of the same symbol or a tendency to mix elements of the two symbols.

Suppose that an ordered sequence contains $m$ first type symbols and $n$ second type symbols. The total number of elements is $m+n = N$. Let $U$ be the total number of runs in the sequence. If the hypothesis is true, then $U$ has an asymptotic normal distribution. The mean of $U$ is $1+2mn/N$ and the standard deviation is $\sqrt{2mn(2mn-N)/N^2(N-1)}$:

$$\begin{aligned} &\Pr\left(\frac{U-1-2mn/N}{\sqrt{\frac{2mn(2mn-N)}{N^2(N-1)}}} \leq z\right) = \Pr(Z \leq z) \\ &= N(z) = \frac{1}{\sqrt{2\pi}} \int_{-\infty}^{z} e^{-\frac{y^2}{2}} dy \end{aligned} \tag{3}$$

For finite sequence size, a continuity correction term 0.5 is introduced to adjust the $z$ statistics as [13]

$$z = \begin{cases} -\frac{U+0.5-1-2mn/N}{\sqrt{\frac{2mn(2mn-N)}{N^2(N-1)}}}, & \text{if} \quad U < 1+2mn/N \\ \frac{U-0.5-1-2mn/N}{\sqrt{\frac{2mn(2mn-N)}{N^2(N-1)}}}. & \text{if} \quad U > 1+2mn/N \end{cases} \tag{4}$$

Intuitively, $U$ has a normal distribution because every arrangement of the two symbols is equally likely to be observed in a random sequence. Its number of runs is mostly likely not too many nor too few. Therefore, if a test sequence has an intermediate value of $U$, the hypothesis is supported. Otherwise, the hypothesis tends to be rejected because of the small likelihood of such event in a random sequence. To state formally, in a randomness test we would like to test the following hypothesis and alternative:

$$\begin{aligned} H: &\quad \text{Sequence is random} \\ A: &\quad \text{Sequence is not random} \end{aligned} \tag{5}$$

A small $z$ in absolute value indicates that the hypothesis is true, while a large $z$ in absolute value would cast doubts on the validity of the hypothesis. Suppose we choose a value $c > 0$ and accept $H$ if $|z| \leq c$, the probability of rejecting $H$ when it is true is:

$$\begin{aligned} &\Pr(\text{Reject } H | H \text{ is true}) \\ &= \Pr(Z > c | H \text{ is true}) + \Pr(Z < -c | H \text{ is true}) \\ &= 2(1 - N(c)). \end{aligned} \tag{6}$$

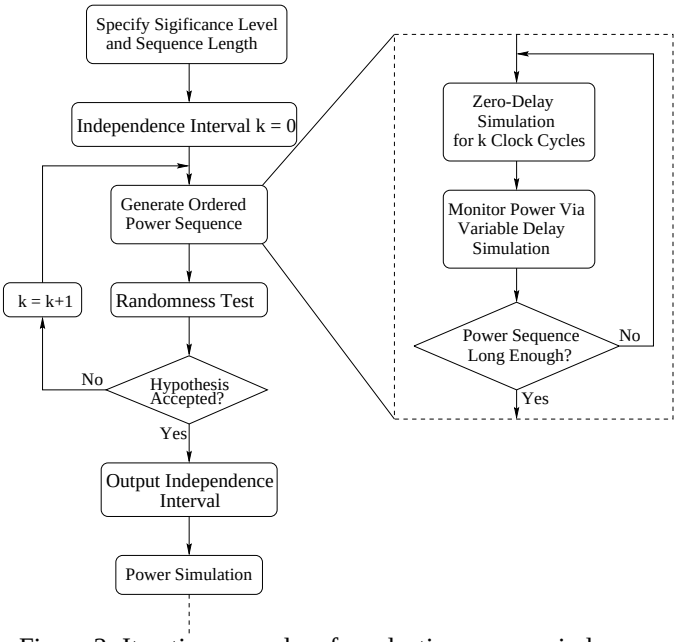


Figure 2: Iteration procedure for selecting a proper independence interval.

Equation (6) holds because $N(z)$ is symmetric. Usually, $c$ is chosen such that (6) has a small value $\alpha$. With $\alpha$ specified, the corresponding $c$ can be found by

$$c = N^{-1}(1 - \frac{\alpha}{2}) \tag{7}$$

$\alpha$ is called the *significance level*. Thus, the randomness test proceeds as follows. Given an ordered sequence of two symbols, count the value of $U$, $m$, $n$, and calculate the value of $z$. Accept the randomness hypothesis with $\alpha$ significance level if $|z| \leq c$. Reject the hypothesis and accept the alternative if $|z| > c$.

### B. Selection of Independence Interval

Since the original runs test only handles sequences of two symbol types, it cannot be directly applied to test the randomness of a power sequence. Given one such sequence, a dichotomizing criterion is to find its median, assign (conceptually) symbol A to all values smaller than the median, and symbol B to the other values. The values of $m$, $n$, $U$ and $z$ can be calculated accordingly to determine the test result with $\alpha$ specified.

Using the randomness test, we develop a sequential procedure to efficiently select a proper independence interval, as depicted in Fig. 2. Initially, the trial interval is set to zero and a power sequence is collected by sampling power dissipation in every clock cycle. The significance of the hypothesis is then evaluated by the test statistic (4) and compared with the user-specified level to determine the test outcome. If the hypothesis is accepted, the power sequence is deemed sufficiently random and an independence interval of zero

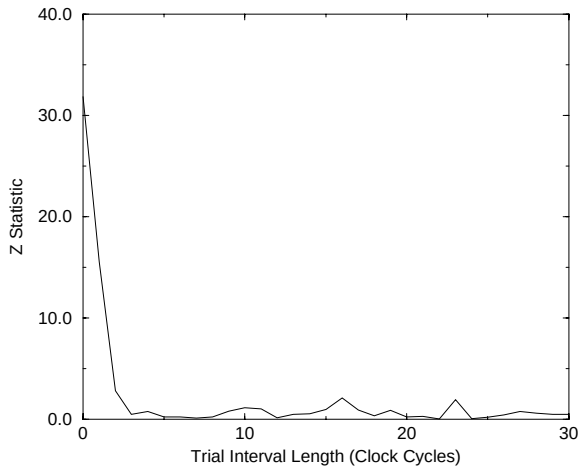


Figure 3: $z$-statistic values as a function of independence inteval length of circuit $s1494$. Power sequence sequence is 10000.

is returned. Otherwise, the trial interval is incremented by one clock cycle to reduce the temporal correlation. A new power sequence is generated such that every two adjacent power data in the sequence are separated by the trial interval, and is tested again. The iteration continues until the hypothesis is accepted. Typically, temporal correlation dissipates fairly fast with increasing trial interval length. As an example, Fig. 3 plots the variation of the $z$-statistic value with the trial interval length for a power sequence of length 10,000 for circuit $s1494$. A small $z$ value indicates higher randomness. It shows that an independence interval of several clock cycles is sufficiently long to generate a random power sample. This observation agrees with the $\phi$-mixing property we assumed previously.

## IV. Estimation of Average Power

The independence interval determined by Fig. 2 is of proper length and can be used to generate a random power sample which is in turn analyzed to estimate average power (please refer to Fig. 1). For the sake of simulation efficiency, a two-phase approach is adopted in random sample generation. During the independence interval, circuit simulation is simply used to reduce the temporal correlation and no power sampling takes place. Thus zero-delay simulation of the next-state logic of the FSM [3] is sufficient. At the end of the independence interval, the observed state vectors and associated input patterns are fed into a general-delay circuit simulator to calculate the power consumption. With a random power sample, a stopping criterion is invoked to measure the convergence and control the sample size. Depending on the desired robustness, one can choose a parametric criterion based on the central-limit theorem [1], or nonparametric ones based on Kolmogorov-Smirnov statistic [6] and order statistics [7], respectively. In this paper, we choose [7] because it provides a good tradeoff between simulation

| Circuit Name | SIM (mW) | $I.I.$ | $\overline{\mu}_p$ (mW) | Sample Size | CPU Time (sec) |
|---|---|---|---|---|---|
| s208 | 0.276 | 2 | 0.276 | 4928 | 138.8 |
| s298 | 0.430 | 2 | 0.429 | 2816 | 73.6 |
| s344 | 0.751 | 1 | 0.751 | 960 | 14.6 |
| s349 | 0.785 | 2 | 0.785 | 1088 | 21.8 |
| s382 | 0.433 | 2 | 0.433 | 2176 | 75.6 |
| s386 | 0.519 | 1 | 0.518 | 1728 | 35.4 |
| s400 | 0.418 | 2 | 0.420 | 2272 | 52.7 |
| s420 | 0.353 | 2 | 0.354 | 4576 | 195.0 |
| s444 | 0.427 | 3 | 0.427 | 2400 | 69.9 |
| s510 | 1.175 | 1 | 1.175 | 3168 | 114.7 |
| s526 | 0.443 | 1 | 0.434 | 2176 | 53.1 |
| s641 | 0.786 | 1 | 0.787 | 1088 | 26.1 |
| s713 | 0.804 | 1 | 0.804 | 1088 | 26.2 |
| s820 | 0.957 | 1 | 0.957 | 1952 | 58.2 |
| s832 | 0.941 | 3 | 0.941 | 2080 | 75.1 |
| s838 | 0.443 | 3 | 0.443 | 2272 | 149.4 |
| s1196 | 3.080 | 1 | 3.079 | 608 | 26.7 |
| s1238 | 3.009 | 0 | 3.010 | 576 | 24.4 |
| s1423 | 2.773 | 1 | 2.774 | 2368 | 275.0 |
| s1488 | 1.844 | 2 | 1.844 | 4000 | 293.0 |
| s1494 | 1.735 | 5 | 1.735 | 3936 | 392.5 |
| s5378 | 6.667 | 2 | 6.659 | 352 | 51.9 |
| s9234 | 2.008 | 1 | 2.008 | 704 | 79.6 |
| s15850 | 5.939 | 1 | 5.938 | 896 | 462.8 |

Table 1: Power estimation results.

accuracy and efficiency [10]. Interested readers are referred to [7] for details of derivation.

## V. Experimental Results and Discussion

The proposed technique has been implemented into our distribution-independent power estimation tool (DIPE). DIPE represents a general power estimation framework. It can be adopted in conjunction with any circuit simulator, depending on the desired simulation accuracy. DIPE has been applied to a set of ISCAS89 sequential benchmark circuits on a SPARC 20 workstation with 244 MB memory. All circuits are assumed to operate at a clock frequency of 20MHz with 5V power supply. The significance level of the randomness test is set to 0.20 while the maximum error allowed was specified as 5% with 0.99 confidence. The signals at primary inputs are assumed to be mutually independent and have probabilities of 0.5. However, correlated input streams can also be handled without any extra work as DIPE does not make assumptions on input pattern statistics. The power sequence length for the randomness test should be carefully selected. It should not be too long because simulation efficiency may be degraded by the search loop for a proper independence interval. Neither can it be too short because statistical fluctuations in hypothesis test results reduce with the test sample size. In the following experiments, the power sequence length is chosen to be 320 because the gain in statistical stability of the test results is marginal if it is any longer.

| Circuit | $II_{min}$ | $II_{max}$ | $II_{avg}$ | $S_{avg}$ | $D_{avg}$ | Err(%) |
|---|---|---|---|---|---|---|
| s208 | 0 | 5 | 1.60 | 5015 | 0.87 | 0.0 |
| s298 | 1 | 2 | 1.60 | 2650 | 1.13 | 0.0 |
| s344 | 1 | 3 | 1.45 | 964 | 0.99 | 0.0 |
| s349 | 1 | 3 | 1.40 | 959 | 1.03 | 0.0 |
| s382 | 0 | 3 | 1.65 | 2247 | 1.14 | 0.0 |
| s386 | 1 | 2 | 1.20 | 1788 | 1.03 | 0.0 |
| s400 | 1 | 4 | 1.85 | 2291 | 1.08 | 0.0 |
| s420 | 0 | 6 | 1.39 | 4265 | 1.25 | 0.9 |
| s510 | 0 | 5 | 1.20 | 3141 | 0.99 | 0.0 |
| s526 | 1 | 3 | 1.20 | 2230 | 1.12 | 0.0 |
| s641 | 0 | 3 | 0.85 | 1077 | 0.96 | 0.0 |
| s713 | 0 | 2 | 0.70 | 1098 | 1.01 | 0.0 |
| s820 | 0 | 2 | 1.20 | 1951 | 1.04 | 0.0 |
| s832 | 0 | 3 | 1.30 | 2044 | 1.03 | 0.0 |
| s838 | 1 | 3 | 1.40 | 2833 | 1.79 | 1.4 |
| s1196 | 0 | 3 | 0.85 | 586 | 0.97 | 0.0 |
| s1238 | 0 | 1 | 0.40 | 567 | 1.00 | 0.0 |
| s1423 | 1 | 3 | 1.60 | 2416 | 1.07 | 0.0 |
| s1488 | 1 | 4 | 2.20 | 4012 | 1.27 | 0.1 |
| s1494 | 1 | 5 | 2.60 | 4009 | 1.14 | 0.0 |
| s5378 | 1 | 10 | 2.40 | 352 | 1.40 | 0.7 |
| s9234 | 1 | 6 | 1.95 | 894 | 0.91 | 0.0 |
| s15850 | 1 | 3 | 1.20 | 900 | 1.15 | 0.0 |

Table 2: Large number simulation summary.

Table 1 shows the power estimation results for the test circuits. In Table 1, SIM is the sample average power obtained from taking the average of power dissipation in 1 million consecutive clock cycles. It is deemed a sufficiently accurate estimate of the real average power, and is used as the reference for all experiments. $I.I.$ is the independence interval determined by the randomness test. The average power estimate $\overline{\mu}_p$ is obtained by taking the average of the sample whose size is listed in column Sample Size. CPU time usage is reported in the last column. From Table 1, several observations can be made. 1) For all test circuits, DIPE produces accurate average power estimates with reasonable amount of CPU time. 2) Usually, an independence interval of a few clock cycles is sufficient for the randomness hypothesis to be accepted with the specified significance level. This observation agrees with [4] on that a small unrolling factor of a FSM is generally enough for accurate power estimation. 3) The duration of the independence interval is determined dynamically and varies with the target circuit. Hence simulation efficiency is greatly improved by not assigning a pessimistic warm-up period *a priori* [9].

To understand the average performance of the proposed technique, we conducted 1,000 simulation runs for every circuit and summarized the results in Table 2. In this table, $I.I._{min}$, $I.I._{max}$ and $I.I._{avg}$ are the minimum, maximum and average independence interval, respectively. $S_{avg}$ is the average sample size and $D_{avg}$ is the average percentage deviation of the estimation results from the reference value. In order to consider the deviation in both polarities, $D_{avg}$ is

estimated by

$$D_{avg} = \frac{1}{N} \sum_{i=1}^{N} \frac{|P_{exact} - P_{estimate}|}{P_{exact}} \times 100\%, \quad (8)$$

where $N$ is the number of simulation runs. In this table, the independence interval varies somewhat because the randomness test provides statistical rather than deterministic conclusion on whether or not the power sequence is "random enough". Thus, for a circuit we would not obtain a fixed independence interval. Nevertheless, Table 2 shows that the estimation results indeed meet the accuracy specification with very low average deviation. The accuracy and robustness of the technique are therefore demonstrated.

## VI. Conclusion

We have proposed a new statistical technique for average power estimation in sequential circuits. Power estimation problem in sequential circuits is more complicated than in combinational circuits because of the feedback mechanism. Power dissipation data in consecutive clock cycles are temporally correlated, violating the basic assumption of all statistical mean inference procedures. Lack of knowledge on the stationary state probabilities of a FSM also makes it difficult to generate meaningful state vectors for power simulation. We overcome these problems by proposing a sequential procedure to dynamically determine a proper independence interval separated by which two power data can be viewed as mutually independent. Random samples can be generated and analyzed by a distribution-independent stopping criterion for user-specified accuracy requirement. The technique has been successfully applied to a set of benchmark circuits with high accuracy and efficiency.

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