Low-Power Design Tools — Where is the Impact?

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Abstract

Power dissipation is rapidly becoming one of the most significant problems in IC design, and this in portables as well as ASIC and high-performance microprocessor platforms. In recent years, we have witnessed the emergence of a variety of design methods and design automation tools to keep dissipation within bounds. This might give the impression that power minimization is a solved issue, both from a design and a design automation perspective.

Unfortunately, the truth is far from that. The next-generation designs are destined to be even more challenging from a power-dissipation perspective and novel solutions will be needed to meet the challenges. This in turn will require innovative EDA tools and methodologies.

This panel, composed of designers, CAD managers and EDA manufacturers, addresses the most compelling issues in low-power low-energy design automation, including what effectively works in the real-world and what does not. The discussion also focuses on what breakthroughs are needed for the next-generation designs.

Panelist Statements

Bill Bell — Texas Instruments, Dallas, TX

In the design era of system-on-a-chip and reusable Intellectual Property (IP) blocks, low-power design issues that were within our control are more difficult to resolve. Before, we could generally squeeze enough power out of the design using special clock gating or lower level gate and transistor sizing methods to meet our goals. We cannot do this anymore since only a small portion of the power comes from our own IP. Now we have to rely on others (even inside your own company) to help meet our power goals.

This drives two major issues that are not being adequately addressed. 1) The planning process for low-power design is as complicated if not more complicated than design planning for timing, yet no low-power design planning tools exist. 2) If we are going to have to rely on others for portions of our designs, then how are we going to communicate our power needs? We need standards for power control on IP. We need standards for specifying power usage, power constraints, power tests, power specs (peak power, RMS power, average power). These standards will help define the usage of power information in the tools in the process like routers, analysis tools, and synthesis tools.

Jerry Frenkil — Sente Inc., Chelmsford, MA

See embedded tutorial.

Vassilios Gerousis—Motorola Inc., Tempe, AZ

The EDA industry has concentrated on power analysis tools, both in the areas of transistor, gate and RTL. Very few companies concentrate on RTL analysis. An evaluation of these tools will be presented at the panel. Very limited amount of work is done at the RTL level for power optimization. Only high-performance designers as well designers of battery-operated devices have concentrated on low-power designs (digital and analog) and EDA tools have not met their demands. Architectural-level tools for power optimization are still at the university laboratory stage.

Massoud Pedram—USC, Los Angeles, CA

It is widely recognized that efficient and accurate power estimation is the key to power minimization in VLSI circuits and systems. There is also a critical need to develop and introduce a power estimation/evaluation methodology which spans various design levels and different design styles. Essential components of such a methodology include: average and peak power estimation tools for ASICs and custom circuits, detailed cell characterization, advanced statistical sampling strategies, probabilistic compaction techniques, cycle-accurate RT-level power macro-modeling, a multi-level simulation environment, and behavioral/informational models of energy dissipation.

Deo Singh — Intel Corp., Santa Clara, CA

Reducing Power through Low Power Design!

Contrary to popular academic beliefs, power reduction will not be achieved through CAD tools alone. While CAD logic synthesis and gate/transistor sizing tools have had respectable but limited impact, the answer to power reduction lies in design techniques. The design techniques must cover all areas of design: architectural/micro-architectural, RTL, logic, circuit & physical design. Academia must focus on developing new efficient low power logic/circuit families. New circuit families must necessarily be elegantly voltage-scalable. In the case of programmable architectures, low-power design techniques must be complemented by software compiler optimizations. Only after design techniques are well understood will it make sense to develop CAD tools.

Jim Sproch — Synopsys, Inc., Mountain View, CA

Power Optimization Rules!

The EDA industry has produced several analysis tools that help designers quantify their power problems, and some optimization tools to quench excess dissipation. More tools are needed; they must fit existing methodologies, and the tools must be internally consistent between analysis and optimization, and across all levels of abstraction. Power problems are often trickier to solve than timing problems because power is more pattern-dependent than timing. Low-power design techniques often conflict with area and timing constraints. Power management is ultimately about optimization tools. Designers require automation to achieve their time-to-market objectives. Analysis should ideally be relegated to a back-end validation step.