



SIGDA Publications on CD-ROM:

DAC '97
Design Automation Conference

Anaheim, CA
June 9 - 13, 1997

DAC97 on CD-ROM Copyright © 1997 by the Association for Computing Machinery, Inc. Permission to make digital or hard copies of part or all of this work is granted without fee provided that copies are not made or distributed for fee or direct commercial advantage, that copies show this notice on the first page or initial screen of a display along with the full citation, and that copies are not posted on public servers. Copyrights for components of this work owned by others than ACM must be honored. Abstracting with credit is permitted. To copy otherwise, to republish, to repost on public lists or servers, or to use any component of this work in other works whether directly or by incorporation by a link, requires prior specific permission and/or a fee. Permissions may be requested from Publications Dept, ACM Inc., 1515 Broadway, New York, NY 10036, fax 212-869-0481, or permissions@acm.org.

ACM Order # 477971

ISBN # 0-89791-847-9

Click on the text below to go to:

Cover Page

Front Matter

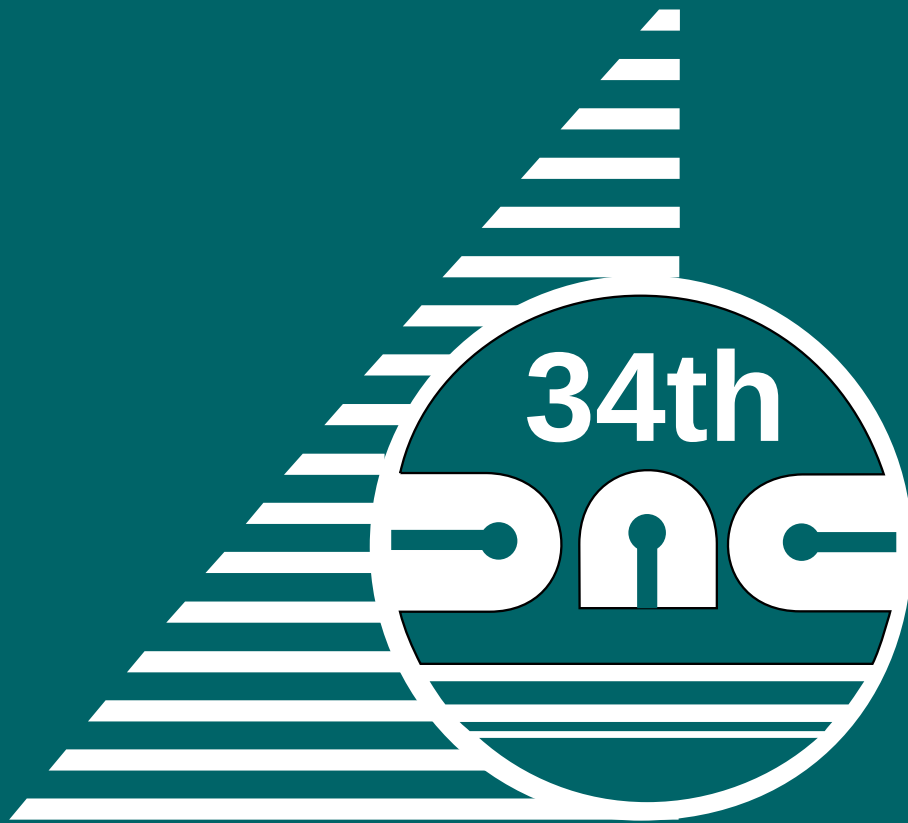
Table of Contents

Session Index

Author Index

PROCEEDINGS 1997

DESIGN AUTOMATION CONFERENCE®



Anaheim, CA

Anaheim Convention Center
June 9 - 13, 1997

Sponsored by



PROCEEDING OF THE 34th DESIGN AUTOMATION CONFERENCE

Copyright ©1997 by the Association for Computing Machinery, Inc. Copying without fee is permitted provided that copies are not made or distributed for direct commercial advantage and credit to the source is given. Abstracting with credit is permitted. For other copying of articles that carry a code at the bottom of the first page, copying is permitted provided that the per-copy fee indicated in the code is paid through the Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923. For permission to republish write to Director of Publications, Association for Computing Machinery, 1515 Broadway, New York, NY 10036. To copy otherwise or republish, requires a fee and/or specific permission.

ACM Order Number 477970
ISBN 0-89791-920-3

IEEE Catalog Number 97CH36101
ISBN 0-89791-920-3 (Softbound Edition)
ISBN 0-7803-4093-0 (Casebound Edition)
ISBN 0-7803-4094-9 (Microfiche Edition)

Library of Congress Number 85-644924

ISSN 0738-100X

Additional copies of 1997 or prior Proceedings may be ordered prepaid from

ACM Order Department
P.O. Box 12114
Church Street Station
New York, NY 10257

ACM European Service Center
108 Cowley Rd.
Oxford, OX41JF, U.K.
Phone: 44-1865-382338
Fax: 44-1865-381338
E-mail: ACM_Europe@acm.org

Phone: 1-800-342-6626
(U.S.A. and Canada)
+1-212-626-0500
(All other countries)
Fax: +1-212-944-1318
E-mail: acmhelp@acm.org

Additional copies of this publication are available from

IEEE Service Center
P.O. Box 1331
445 Hoes Lane
Piscataway, NJ 08855-1331

1-800-678-IEEE
1-908-981-1393
1-908-981-9667 (Fax)
833-233 (Telex)

General Chair's Welcome

Welcome to the 34th Design Automation Conference!

DAC is the premier forum for exchanging your most exciting ideas and innovations in design automation. At DAC you will hear about the latest research and development in design tools. You will also hear about designers' experiences with design automation, good and bad. They will tell you what their hottest designs are—and how they designed them. Combined with visionary keynote addresses, 170 exhibits, 7 full-day tutorials and numerous other special technical gatherings, the technical program represents the very best of the leading edge technology driving the world's integrated circuit and electronic systems industry.

These proceedings, representing an outstanding expanded technical program were assembled under the very able direction of Technical Program Co-Chairs Giovanni De Micheli (Design Tools) and Jan Rabaey (Design Methods). Nearly 400 papers from North America, Europe, the Middle East, Asia and the South Pacific were submitted to the design tools and design methods tracks, and were reviewed by over 700 professionals. The Technical Program Committee used these reviews, along with their own expert opinions, to select the very best 139 papers in topics ranging from deep submicron design to hardware-software co-design. Nine panel sessions, including EDA company CEOs' views of their industry, challenges in worldwide intellectual property reuse, and financing EDA startups, complement the technical presentations and tutorials embedded in the 5 tracks of the technical program.

I want to thank all of the people who contributed to the success of DAC: the Executive Committee, the Technical Program Committee, the EDA Industry Committee, DAC's sponsors, MP Associates, and especially the exhibitors, authors, speakers, session organizers and session chairs. Their hard work and dedication have made this the world's premier conference for electronic design automation tools and methods. DAC is sponsored by ACM/SIGDA, IEEE Circuits and Systems Society, and EDAC. Their members represent the spectrum of DAC's participants and we are thankful for their continued and active support.

Welcome to Anaheim and the 34th Design Automation Conference. See the challenge and promise of electronic design—it has no boundaries. We wish you a very productive and fun-filled week and trust you will find these proceedings to be a valuable information reference for many years to come.

Ellen J. Yoffa

General Chair, 34th Design Automation Conference

EXECUTIVE COMMITTEE

GENERAL CHAIR

Ellen J. Yoffa
IBM Corp.
T.J. Watson Research Ctr.
Rm. 33-109, P.O. Box 218
Yorktown Heights, NY 10598
(914) 945-3270
yoffa@watson.ibm.com

VICE CHAIR

Basant R. Chawla
Lucent Technologies
283 King George Rd., E4D43
Warren, NJ 07059
(908) 559-5281
bchawla@lucent.com

TECHNICAL PROGRAM CO-CHAIR, DESIGN TOOLS

Giovanni De Micheli
Stanford Univ.
Gates Computer Science Bldg.
Rm. 333
Stanford, CA 94305-9030
(415) 725-3632
nanni@galileo.stanford.edu

TECHNICAL PROGRAM CO-CHAIR, DESIGN METHODS

Jan M. Rabaey
Univ. of California
Dept. of EECS, 511 Cory Hall
Berkeley, CA 94720
(510) 643-8206
jan@eecs.berkeley.edu

FINANCE CHAIR

Mary Jane Irwin
Penn State Univ.
Dept. of CS and Engr.
220 Pond Lab.
University Park, PA 16802-6106
(814) 865-1802
mji@cse.psu.edu

TUTORIAL CHAIR

Stephen Trimberger
Xilinx, Inc.
2100 Logic Dr.
San Jose, CA 95124
(408) 879-5061
steve.trimberger@xilinx.com

ELECTRONIC SYSTEMS INDUSTRY CHAIR

Bryan Preas
Xerox PARC
3333 Coyote Hill Rd.
Palo Alto, CA 94304
(415) 812-4845
preas@parc.xerox.com

EDA INDUSTRY CHAIR

Michael Lorenzetti
Mentor Graphics Corp.
8005 SW Boeckman Rd.
Wilsonville, OR 97070-7777
(503) 685-1258
mike_lorenzetti@mentorg.com

ELECTRONIC MEDIA CHAIR

Randal Bryant
Carnegie Mellon Univ.
School of Computer Science
Pittsburgh, PA 15213
(412) 268-8821
randy.bryant@cs.cmu.edu

PUBLICITY CHAIR

Abbie Kendall
OrCAD
9300 SW Nimbus Ave.
Beaverton, OR 97008
(503) 671-9500
abbie@orcad.com

EXECUTIVE COMMITTEE (cont.)

EUROPE/MIDDLE EAST REPRESENTATIVE

Gerry Musgrave
Brunel Univ.
Dept. of EEE
Uxbridge, UB8 3PH, UK
(44) 1-895-203-251
gerry@ahl.co.uk

PAST-CHAIR

Thomas P. Pennino
Lucent Technologies, Bell Labs.
101 Crawfords Corner Rd.
Rm. 1M-415
Holmdel, NJ 07733
(908) 949-7340
tpennino@lucent.com

ACM REPRESENTATIVE

James Cohoon
Univ. of Virginia
Dept. of Computer Science
Olsson Hall
Charlottesville, VA 22903
(804) 982-2210
cohoon@virginia.edu

ASIA/INDIA/S. PACIFIC REPRESENTATIVE

Fumiyasu Hirose
Fujitsu Labs. Ltd.
CAD Lab.
4-1-1 Kamikodanaka, Nakahara-ku
Kawasaki 211, Japan
(81) 44-754-2663
hirose@flab.fujitsu.co.jp

IEEE/CAS REPRESENTATIVE

Philip Lopresti
Private Consultant
327 Sked St.
Pennington, NJ 08534
(609) 737-2445
pvl@nec1.nec.com

EDAC REPRESENTATIVE

Lorie Bowlby
Precedence, Inc.
1700 Dell Ave.
Campbell, CA 95008
(408) 341-4275
lorie@precedence.com

EXHIBIT MANAGER

Marie R. Pistilli
MP Associates, Inc.
5305 Spine Rd., Ste. A
Boulder, CO 80301
(303) 530-4562
marie@dac.com

CONFERENCE MANAGER

P.O. Pistilli
MP Associates, Inc.
5305 Spine Rd., Ste. A
Boulder, CO 80301
(303) 530-4562
pat@dac.com

Technical Program Committee

Giovanni De Micheli
Design Tools Co-Chair
Stanford Univ.
Gates Computer Science Bldg.
Rm. 333
Stanford, CA 94305-9030
(415) 725-3632
nanni@galileo.stanford.edu

Jan M. Rabaey
Design Methods Co-Chair
Univ. of California
Dept. of EECS
511 Cory Hall
Berkeley, CA 94720
(510) 643-8206
jan@eecs.berkeley.edu

David Blaauw
Motorola, Inc.
Bridgepoint Plaza 1
5918 W. Courtyard Dr., Ste. 330
Austin, TX 78730
(512) 794-4356
blaauw@adtx.sps.mot.com

Antun Domic
Synopsis, Inc.
700 E. Middlefield Rd.
Mountain View, CA 94043-4033
(415) 962-5000

Ivo Bolsens
IMEC
VSDM/DISTA
Kapeldreef 75
B-3001 Leuven, Belgium
(32) 16-281-211
bolsens@imec.be

Phil Duncan
Angeles Design Systems
501 Santa Monica Blvd., Ste. 701
Santa Monica, CA 90401
(310) 443-3245
duncan@angeles.com

Raul Camposano
Synopsis, Inc.
700 E. Middlefield Rd.
Mountain View, CA 94043-4033
(415) 694-1769
raul@synopsys.com

Anders Forsen
Ericsson Radio Systems AB
RCUR-T/N
KISTA
16480 Stockholm, Sweden
(46) 8-7572-541
anders.forsen@era-t.ericsson.se

Anantha Chandrakasan
Massachusetts Inst. of Tech.
Dept. of EE, Rm. 38-107
50 Vassar St.
Cambridge, MA 02139
(617) 258-7619
anantha@mtl.mit.edu

Robert C. Frye
Lucent Technologies, Bell Labs.
700 Mountain Ave.
Rm. 1C-339
Murray Hill, NJ 07974-0636
(908) 582-5353
rcf@lucent.com

Nanette Collins
Consultant
37 Symphony Rd., Unit A
Boston, MA 02115-4004
(617) 437-1822
nanette@nvc.com

Patrick Groeneveld
Compass Design Automation
1865 Lundy Ave.
MS 430
San Jose, CA 95131
(408) 434-7601
patrickg@compass-da.com

Jason Cong
Univ. of California
Dept. of CS
4711 Boelter Hall
Los Angeles, CA 90095
(310) 206-2775
cong@cs.ucla.edu

Rajesh K. Gupta
Univ. of California
Dept. of ICS, 208B IERF
Irvine, CA 92697-3425
(714) 824-8052
rgupta@cs.uiuc.edu

Technical Program Committee (cont.)

Randolph E. Harr
DARPA/ETO
3701 N. Fairfax Dr.
Arlington, VA 22203-1714
(703) 696-2253
rharr@darpa.mil

Takahide Inoue
Sony
530 Cottonwood Dr.
Milpitas, CA 95035
(408) 955-4269
inoue@ssl.sel.sony.com

Andrew B. Kahng
Univ. of California
Dept. of CS
3713 Boelter Hall
Los Angeles, CA 90095-1596
(310) 206-7073
abk@cs.ucla.edu

David Ku
Escalade Corp.
2575 Augustine Dr.
Santa Clara, CA 95054
(408) 654-1617
ku@escalade.com

Andreas Kuehlmann
IBM Corp.
T.J. Watson Research Ctr.
P.O. Box 218
Yorktown Heights, NY 10598
(914) 945-3458
kuehl@watson.ibm.com

Luciano Lavagno
Politecnico di Torino
Dipartimento di Elettronica
Corso Duca Degli Abruzzi 24
10129 Torino, Italy
(39) 11-5644150
lavagno@polv2k.polito.it

Sharad Malik
Princeton Univ.
Dept. of EE
Princeton, NJ 08544
(609) 924-8810
sharad@ee.princeton.edu

Alan Mantooth
Analogy, Inc.
P.O. Box 1669
Beaverton, OR 97075-1669
(503) 626-9700
alan@analogy.com

Teresa Meng
Stanford Univ.
Gates Computer Science Bldg., Rm. 301
Stanford, CA 94028
(415) 725-3636
meng@mojave.stanford.edu

Mike Murray
Acuson Corp.
1220 Charleston Rd.
Box 7393
Mountain View, CA 94043
(415) 694-5876
mikem@acuson.com

Kunle Olukotun
Stanford Univ.
Gates Computer Science Bldg., Rm. 302
Stanford, CA 94305-9030
(415) 725-3713
kunle@ogun.stanford.edu

Hidetoshi Onodera
Kyoto Univ.
Dept. of Electronics & Comm.
Sakyo-ku
Kyoto 606-01, Japan
(81) 75-753-5314
onodera@kuee.kyoto-u.ac.jp

Massoud Pedram
Univ. of Southern California
Dept. of EE-Systems
3740 McClintock Ave.
Los Angeles, CA 90089-2562
(213) 740-4458
massoud@zugros.usc.edu

Janusz Rajski
Mentor Graphics Corp.
8005 SW Boeckman Rd.
Wilsonville, OR 97070-7777
(503) 685-4797
rajski@wv.mentorg.com

Technical Program Committee (cont.)

James A. Rowson
Alta Group of Cadence Design Systems, Inc.
555 N. Matilda Ave.
Sunnyvale, CA 94086
(408) 523-4157
jimr@altagroup.com

Karem A. Sakallah
Univ. of Michigan
2213 EECS Bldg.
Ann Arbor, MI 48109-2122
(313) 936-1350
karem@eecs.umich.edu

Gabriele Saucier
Inst. Nat'l Polytech de Grenoble/CSI
46, Ave. Felix Viallet
38031, Grenoble, France
(33) 76-57-46-87
saucier@imag.fr

Deo Singh
Intel Corp.
2200 Mission College Blvd.
MS SC9-13, P.O. Box 58119
Santa Clara, CA 95052-8119
(408) 765-6380
deo_s_singh@ccm.sc.intel.co

Richard Smith
Cadence Design Systems, Inc.
5215 N. O'Connor Rd.
Ste. 1000
Irving, TX 75039
(972) 889-0033
dsmith@cadence.com

Fabio Somenzi
Univ. of Colorado
Dept. ECE, C.B. 425
Boulder, CO 80309-0425
(303) 492-3466
fabio@colorado.edu

Haruyuki Tago
Toshiba America Electronic Components
1060 Rincon Cir.
San Jose, CA 95131
(408) 526-2701
tagoh@taec.com

Vivek Tiwari
Intel Corp.
2200 Mission College Blvd.
M/S-RNB 5-09
Santa Clara, CA 95052
(408) 765-6555
vivek@ee.princeton.edu

Kazutoshi Wakabayashi
NEC Corp.
C&C Research Labs.
4-1-1 Miyazaki
Kawasaki 216, Japan
(81) 44-856-2134
wakaba@sbl.cl.nec.co.jp

Neil Weste
Macquarie Univ.
Electronics Dept.
Sydney 2109, Australia
(61) 2-850-9149
new@mpce.mq.edu.au

Jacob K. White
Massachusetts Inst. of Tech.
Dept. of EECS
Rm. 36-817, 50 Vassar St.
Cambridge, MA 02139
(617) 253-2543
white@mit.edu

Andrew T. Yang
Avant! Corp.
1208 E. Arques Ave.
Sunnyvale, CA 94086-5401
(408) 523-8834
andrew_yang@avanticorp.com

Yervant Zorian
LogicVision, Inc.
31B Chicopee Dr.
Princeton, NJ 08540
(609) 497-1744
zorian@lvision.com

1997 Best Paper Award

This year, awards are made for the best papers in four categories. Winners are determined from detailed reviews of the accepted papers in the technical sessions. Each award is accompanied by a plaque and a cash award of \$400. The awards are given by ACM/SIGDA (Special Interest Group on Design Automation), IEEE/CAS (Institute of Electrical and Electronics Engineers/Circuits and Systems Society) and EDAC (Electronic Design Automation Companies).

PHYSICAL DESIGN AND LOGIC SYNTHESIS

Paper 1.1: "An Improved Algorithm for Minimum-Area Retiming"
Authors: Naresh Maheshwari, Sachin Sapatnekar
Affiliation: Iowa State Univ., Ames, IA

HIGH-LEVEL SYNTHESIS, VERIFICATION AND CODESIGN

Paper 16.2: "Equivalence Checking Using Cuts and Heaps"
Authors: Andreas Kuehlmann, Florian Krohm
Affiliation: IBM Corp., Yorktown Heights, NY

MODELING, SIMULATION AND ESTIMATION

Paper 17.1: "Time-Domain and Mixed Frequency-Time Algorithms for Strongly Nonlinear Circuits with Multi-Tone Excitations"
Author: J.S. Roychowdhury
Affiliation: Lucent Technologies, Bell Labs., Murray Hill, NJ

DESIGN METHODOLOGY

Paper 49.1: "Computer-Aided Design of Free-Space Opto-Electronic Systems"
Authors: S.P. Levitan, T.P. Kurzweg, P.J. Marchand, C. Fan,
M.A. Rempel, D.M. Chiarulli F.B. McCormick
Affiliation: Univ. of Pittsburgh, Pittsburgh, PA Univ. of California, La Jolla, CA

Advancement in Computer Science and Electrical Engineering Undergraduate Scholarships

The objective of the ACSEE Scholarship program is to increase the pool of professionals in Electrical Engineering and Computer Science from under-represented groups (Women, African American, Hispanic, Native American, and Physically Challenged). In 1989, ACM Special Interest Group on Design Automation (SIGDA) began providing the program. Beginning in 1993, the Design Automation Conference provides the funds for the scholarship and SIGDA continues to administer the program for DAC. DAC funds two \$4000 scholarships renewable up to 5 years to graduating high school seniors. The former International Daisy User Group funds one \$1000 one-time-only scholarship.

The 1997 winners will be announced at the Conference. The 1996 winners were:

1996 DAC/IDUG ACSEE Undergraduate Scholarships

DAC \$4K: Ann Nuñez Alejandro, Houston, TX - attending University of Houston

DAC \$4K: Ellen Weiss Carvill, Milford, NY - attending Carleton College

IDUG \$1K: Shawn P. Koch, Houston, TX - attending Rice University

This year, the graduates of the ACSEE program include Hector Villalobos who will be receiving his BS in Electrical Engineering from Santa Clara University and Sung Jo who will receive his BS in Electrical Engineering from San Jose State University.

For more information about the ACSEE scholarship, please contact Dr. Cherrice Traver, EE/CS Department, Union College, Schenectady, NY 12308 email: traverc@doc.union.edu.

CALL FOR PAPERS

35th DESIGN AUTOMATION CONFERENCE®

MOSCONE CENTER • JUNE 15 - 19, 1998

DAC is the premier conference devoted solely to the field of Design Automation. All aspects of the use of computers as aids to the design process are welcome, from conceptual design to manufacturing. Five types of submissions are invited: regular papers, special topic sessions, panels, tutorials, and design contest entries. All types of submissions should be sent to the Program Chair, postmarked NO later than October 10, 1997.

TOPICS OF INTEREST

Authors are invited to submit original technical papers describing recent and novel research or engineering developments in all areas of design automation. The DESIGN TOOLS TRACK (T) is devoted to contributions to the research and development of design tools and the supporting algorithms. The DESIGN METHODS TRACK (M) deals with contributions to the research and development of design methodologies and applications of design automation tools to designs. Topics of interest include, but are not limited to:

DESIGN TOOLS TRACK:

- T1.1 Electrical-level circuit and timing simulation
- T1.2 Discrete simulation
- T1.3 Critical path analysis and timing verification
- T1.4 Power estimation
- T2.1 Testing, fault modeling and simulation, TPG, test validation and DFT
- T2.2 Design and implementation verification (excluding layout verification)
- T3.1 Floorplanning and placement
- T3.2 Global and detailed routing
- T3.3 Module generation and compaction, transistor sizing and cell library optimization, layout verification
- T4.1 Technology independent, combinational logic synthesis
- T4.2 Technology dependent logic synthesis, library mapping, interactions between logic design and layout
- T4.3 Sequential logic synthesis and optimization
- T4.4 High-level synthesis
- T4.5 Asynchronous logic synthesis
- T5.1 Hardware Description Languages
- T5.2 Hardware/Software co-design, partitioning, system-level specification and design aids
- T5.3 Software synthesis and retargetable compilation
- T5.4 Hardware/Software co-simulation
- T6.1 Interconnect and packaging modeling and extraction
- T6.2 Signal integrity and reliability analysis
- T6.3 Analog and mixed-signal design tools
- T6.4 Microsensor and microactuator design tools
- T6.5 Statistical design and yield maximization
- T7.1 Frameworks, intertool communication, WWW-based tools and databases

DESIGN METHODS TRACK:

The Design Methods track deals with innovative methodologies for the design of electronic circuits and systems, as well as creative experiences with design automation in state-of-the-art designs. Submissions for this track will be judged especially on their design application contents.

M1 Design methodologies and case studies for specific design tasks

- M1.1 Design entry and specification
- M1.2 Simulation, analysis, modeling and estimation
- M1.3 Verification, test and debugging
- M1.4 Physical design, module generation, design for manufacturing
- M1.5 Logic and high-level synthesis
- M1.6 System-level design, embedded-system design and co-design
- M1.7 Other

M2 Design flows and case studies for specific application domains and platforms

- M2.1 Board and MCM
- M2.2 FPGA, rapid prototyping and reconfigurable computing
- M2.3 ASIC
- M2.4 Microprocessor, multiprocessor and networking
- M2.5 Multimedia and consumer
- M2.6 DSP, communications and wireless
- M2.7 Other (automotive, medical, optical, ...)

M3 Design technologies and technology drivers

- M3.1 Deep sub-micron: signal integrity, interconnect
- M3.2 High-performance design: timing, clocking and power distribution
- M3.3 Low power design

Watch the WWW for updates! (<http://www.dac.com>)



- M3.4 Mixed-signal, analog, and RF
- M3.5 New devices, sensors, MEMS
- M3.6 Other

M4 Integration and management of DA systems

- M4.1 Management of DA systems, design interfaces
- M4.2 Standardization issues
- M4.3 Distributed, networked, and collaborative design
- M4.4 Intellectual property, design reuse and design libraries

REQUIREMENTS FOR SUBMISSION OF PAPERS

Previously published papers, including workshop proceedings, will not be considered. Each submission should include one cover page and eleven (11) stapled copies of the complete manuscript.

The one cover page should include:

- Name, affiliation, and complete address for each author
- A designated contact person including his/her telephone number, fax number, and email address
- A designated presenter, should the paper be accepted
- A list of topic numbers preceded by the letter T (Tools Track) or M (Methods Track), **ordered by relevancy**, most clearly matching the content of the paper
- The following signed statement: "All appropriate organizational approvals for the publication of this paper have been obtained. If accepted, the author(s) will prepare the final manuscript in time for inclusion in the Conference Proceedings and will present the paper at the Conference."

To permit a blind review, do not include name(s) or affiliation(s) of the author(s) on the manuscript. Include:

- Title of paper
- 60-word abstract indicating significance of contribution.
- The complete text of the paper in English, including all illustrations and references, not exceeding 4000 words. The papers will be reviewed as finished papers. Preliminary submissions will be at a disadvantage.

Notice of acceptance will be mailed to the contact person by February 23, 1998. Authors of accepted papers must sign a copyright release form.

PANELS, TUTORIALS, SPECIAL TOPIC SESSIONS

Proposals should not exceed two pages in length and should describe the topic and intended audience. They must include a list of all participants, including the moderator for Panels. **For proposal instructions, send a one-line email message to proposals@dac.com.**

Special Topic Sessions may be either independent papers with a common theme or a set of closely related papers describing an overall system. In both cases, independent reviews of each paper and evaluation of the session as a whole will be used to select sessions. Proposals for Special Topic Sessions should be submitted **along with the list of papers to be included in the session** and should describe the session's theme. These proposals and paper submissions must be postmarked no later than October 10, 1997.

UNIVERSITY DESIGN CONTEST

Submissions of original electronic designs (circuit or system), developed at universities and research organizations after June 1996 and resulting in operational implementations are invited. Submissions should contain the title of the project, a 60-word abstract and a complete description of the design, not exceeding 4000 words in text. The submission should clarify the originality, distinguishing features, and the measured performance metrics of the design. Proof-of-implementation in the form of die or board photographs and measurement data is a must. Submitted designs should not have received awards in other contests. Submissions will be reviewed by a special committee of experts. Selected designs will be presented and exhibited at the conference.

PROGRAM CHAIR

sponsored by:

MP Associates, Inc.
ATTN: Technical Program Co-Chairs
Jan Rabaey/Randal Bryant
5305 Spine Rd., Suite A
Boulder, CO 80301
For information call: (303) 530-4333



Design Automation Conference Graduate Scholarships

Each year the Design Automation Conference sponsors several \$12,000 scholarships to support graduate research and study in Design Automation (DA), with emphasis in "design and test automation of electronic and computer systems". Each scholarship is awarded directly to a university for the Faculty Investigator to expend in direct support of one or more DA graduate students.

The criteria for granting such a scholarship expanded in 1996 to include financial need. The criteria are: the academic credentials of the student(s); the quality and applicability of the proposed research; the impact of the award on the DA program at the institution; and financial need. Preference is given to institutions that are trying to establish new DA research programs.

Information on next year's DAC scholarship award program will be available on the DAC World Wide Web page at: <http://www.dac.com/scholarship.html>.

Design Automation Conference Graduate Scholarship Awards

- Prof. R. Iris Bahar of the Brown University, Providence, RI, for Qian Cui. Their project is entitled, "Using Implications to Drive Low-Power Optimization of Technology-Dependent Circuits".
- Prof. David Kaeli of the Northeastern University, Boston, MA, for Ying Liu. Their project is entitled, "Designing in the 3rd Dimension".
- Prof. Miodrag Potkonjak of the University of California, Los Angeles, CA, for Inki Hong. Their project is entitled, "Design Methodology for Synthesis of Real-Time Systems on Silicon".
- Prof. Shambhu J. Upadhyaya of the State University of New York, Buffalo, NY, for Kamran Zarrineh. Their project is entitled, "A Design for Test Perspective on Memory Synthesis".

The Lucent Technologies supported DAC Graduate Scholarship is awarded to:

- Prof. Sachin S. Sapatnekar of the Iowa State University, Ames, IA, for Naresh Maheshwari and Yanbin Jiang. Their project is entitled, "Practical Methods for Gate-Level and Transistor-Level Timing Optimization".

The Xilinx supported DAC Graduate Scholarship is awarded to:

- Prof. Michael J. Alexander of the Washington State University, Pullman, WA, for Yongmin Ge. Their project is entitled, "CAD-Driven FPGA Architecture Design".

Design Automation Conference Graduate Scholarship Committee

The 1997 DAC Scholarship Committee was comprised of the following people:

James P. Cohoon, University of Virginia (Chair)
Philip V. Lopresti, Independent Consultant
Jeffrey S. Salowe, Cadence Design Systems, Inc.

1997 SIGDA Meritorious Service Award

Robert A. Walker
Kent State University
Kent, OH

REVIEWERS

A total of 389 manuscripts were submitted to the 1997 DAC. The Conference Executive and Technical Program Committees wish to acknowledge the time and effort spent by the following people who reviewed these manuscripts and returned the review forms completed. Our thanks to all of those who participated and contributed to the success of the Conference.

David G. Agnew	Daniel Brand	Brian V. Chess
Vishwani Agrawal	Daniel R. Brasen	Chun-Ping George Chi
Aharon Aharon	Ansgar Bredenkeld	Anton V. Chichkov
Robert Aitken	Forrest D. Brewer	Pai Chou
Salahuddin Almajdoub	Jay B. Brockman	Malgorzata Chrzanoska-Jeske
Wafa Almansoori	Richard B. Brown	Johan Cockx
Charles J. Alpert	Randal E. Bryant	John M. Cohn
Joachim Altmeyer	Joseph Buck	Bob Conn
N.R. Aluru	Thomas Buechner	Alan J. Coppola
Tod Amon	Giacomo Buonanno	Tedd Corman
Catia Marc Angelo	Timothy M. Burks	Fulvio Corno
Kurt Antreich	Gianpiero Cabodi	Jose Luis Correia Neves
Rafael Aquino	Paolo E. Camurati	Olivier R. Coudert
Mario Aranha	Ariel Cao	Ajay J. Daga
Guido Araujo	Wanlin Cao	Joseph P. Damore
Pranav Ashar	Juan Antonio Carbalo	Sumit Dasgupta
William W. Au	Joan E. Carletta	Hiroshi Date
Michael S. Austwick	Robert Carragher	Kaushik De
Bechir Ayari	Patrizia Cavalloro	Gjalt De Jong
Smita Bakshi	Viraphol Chaiyakul	Aykut Dengi
Felice Balarin	K. Chakrabarty	Allen M. Dewey
Erich Barke	Abhijeet Chakraborty	Lewis W. Dewey
John K. Bartholomew	Tapan J. Chakraborty	Sujit Dey
Eugene Beaumont, Jr.	Sreejit Chakravarty	Olivier Deygas
James A. Beausang	Heming H. Chan	Abhijit Dharchoudhury
James E. Beck	V. Chandramouli	Thomas E. Dillinger
Dirk Behrens	K.C. Chang	Cuong H. Do
Jeff Bell	Yao-Wen Chang	Enrico Domenis
Luca Benini	Basant Chawla	Bernard J. Doray
Alfredo Benso	Chien-In Henry Chen	Rolf Drechsler
Michel Berkelaar	Chih-Ang Chen	Anthony D. Drumm
E. Berrebi	Chih-Tung Chen	Philippe P. Duchene
Mike A. Beunder	Dahe Chen	Nikil D. Dutt
Narasimha Bhat	Howard H. Chen	Amir H. Earrahi
Sandeep Bhatia	Sao-Jie Chen	Klaus Eckl
Subhrajit Bhattacharya	Wenfeng Chen	Hisakazu Edamatsu
Flavio Bianchi	Xiangfeng Chen	Stephen A. Edwards
Peter Bingley	Xinghao Chen	Avi Efrati
Stephen Blythe	Yirng-An Chen	Cindy Eisner
Richard Booth	David I. Cheng	Ibrahim M. Elfadel
Carsten Borchers	Wei-Kai Cheng	Norman Elias
Bhaskar Bose	Wu-Tung Cheng	Peter J.H. Elias
Eric Bracken	Yi-Kan Cheng	Frank Eloff

Nong Fan
Erin P. Fassio
Gary K. Fedder
Peter Feldmann
Gerard Fenelon
Fabrizio Ferrandi
Josef Fleischmann
Paulo Flores
Marie-Lise Flottes
Paul Franzon
Mark S. Fredrickson
Stephen T. Frezza
Thomas Fuhrman
Hiroshige Fujii
Takashi Fujii
Masahiro Fujita
Tomoo Fukazawa
F. Fummi
George Gadelkarim
Anthony J. Gadiant
Dinesh D. Gaitonde
Shantanu Ganguly
Andreas Ganz
David S.-W. Gao
Daniel Geist
Dimitris Gizofoulos
Nanda Gopal
Nobuyuki Goto
Ravender Goyal
Robert B. Grafton
Werner Grass
Gary S. Greenstein
Thorsten Groetker
J.P. Grossman
John S. Grout
Lon Grover
Aarti Gupta
Rohini Gupta
Mircba R. Gusat
Paul Gutwin
Ian A. Guyler
John Hagerman
Winfried F. Hahn
Ibrahim N. Hajj
Cordula Hansen
Justin Harlow
Ismed D. Hartanto
Soha Hassoun
Lei He

Jim Heaton
Lars Hedrich
Richard Heidenreich
Shankar Hemmady
Stefan Hendricx
Manfred Henftling
Harry Hengster
Hiroyuki Higuchi
Dwight D. Hill
Lynwood Hines
Kanji Hirabayshi
Mark J. Hirsch
Pei-Hsin Ho
Shervin Hojat
Ulrich Holtmann
Inki Hong
Seong K. Hong
Wei Hong
Yatin V. Hoskote
Michael S. Hsiao
Harry Hsieh
Yaun-Chung Hsu
Alan J. Hu
Xiaobo Hu
Shi-Yu Huang
Ying-Min I. Huang
Yunching Huang
Michael Hutton
Yean-You Hwang
C. Norris Ip
Quan Iran
Mary Jane Irwin
Balakrishnan Iyer
James Jacob
Neil G. Jacobson
Margarida Jacome
Alok Jain
Michael A. Jassowski
Alvin Jee
James Jensen
Jochen AG Jess
Bruce D. Jilek
Frank M. Johannes
Eric N. Johnson
Eric W. Johnson
K.D. Jones
Luli Josephson
Raju Joshi
Jing-Yang Jou

Hsiao Juan
Knut Just
Hilary J. Kahn
Asawaree Kalavade
Takashi Kambe
Steve Kang
De-Yu Kao
William H. Kao
Arvind K. Karandikar
Osamu Karatsu
Ireneusz Karkowski
Maddumage Karunaratne
Mark A. Kassab
Masahiro Kawakita
M. Kawarabayashi
Wuudiann Ke
Holger Keding
Martin Keim
Pratibha Kelapure
Kevin J. Kerns
John E. Kerro
Manpreet Khaira
Sanjay A. Khan
Sunil Khatri
Kei-Yong Khoo
Robert H. Klenke
Alfred Koelbl
Marcel Kolsteren
Srinivas Komar
Alex Kondratyev
Andrzej Krasniewski
Byron Krauter
Harish Kriplani
Kayhan Kucukcakar
Yuji Kukimoto
David S. Kung
Wolfgang Kunz
Arno Kunzmann
Ming-Ter Kuo
Sy-Yen Kuo
William K. Lam
Dirk Lanneer
Chunho Lee
Jaushin Lee
Jayhyun Lee
Jens Leenstra
Christian Legl
Gunther Lehmann
Daksh Lehter

Guang-Tsai Lei
Rainer Leupers
Regis Leveugle
Moshe Levinger
Steven Levitan
Jeremy R. Levitt
Jian Li
Jianmin Li
Mien Li
Yau-Tsun Steven Li
Ying-Meng Li
Stan Liao
Luigi Licciardi
Clifford Liem
Chih-Chang Lin
David Ling
Paul E. Lippens
Yu Liu
Arun N. Lokanathan
David E. Long
Michael Lorenzetti
Aiguo Lu
Enrico Macii
Christophe Madre
Rafic Z. Makki
Enrico Malavasi
Joseph Malka
Srilatha Manne
Elena Marchetti
Diana Marculescu
Radu Marculescu
Grant E. Martin
Peter Marwedel
Masataka Matsui
Yusuke Matsunaga
Peter Maurer
Peter C. Maxwell
Uwe B. Meding
Mahesh Mehendale
Sharad Mehrotra
Gaurav Mehta
Huzefa A. Mehta
Noel Menezes
Scott F. Midkiff
Paolo Miliozzi
Linda Milor
Shin-ichi Minato
Takashi Mitsuhashi
Manmohan Mittal

Hiroshi Miyashita
Toshiaki Miyazaki
Peter Moceyunas
Paul Molitor
Delfin Y. Montuno
Jean Paul Moriw
Seijiro Moriyama
Vasily G. Moshnyaga
Chandra S. Moturu
Klaus D. Mueller-Glaser
Pradipto Mukherjee
Rajarshi Mukherjee
Fidel Muradali
Masami Murakata
Michiaki Muraoka
Gerry Musgrave
Benoit Nadeau-Dostie
Surendra Nahar
Yuichi Nakamura
J. Narasimhan
Sridhar Narayanan
Violante Nassimo
Danial Neebel
M. Nemani
Seiichi Nishio
Lisa M. Noack
Istvan Novak
Ramakrishna Nunna
Peter Odryna
Jaewon Oh
Yukihito Oowaki
Neven Orhanovic
David Z. Pan
Peichen Pan
Wenwei Pan
Preeti Ranjan Panda
Rajendran V. Panda
Maurizio Paolini
Christos Papachristou
Marios C. Papaefthymiou
Abelardo Pardo
Rubin A. Parekhji
Keshab K. Parhi
Janak H. Patel
Srinivas Patil
Lalit M. Patnaik
Michael Payer
Stefan Pees
Marc Picquendar

Lawrence T. Pileggi
Carl P. Pixley
Francois Pogodalla
Franck J. Poirot
Massimo Poncino
Guido Post
Miodrag M. Potkonjak
Dhiraj K. Pradhan
John Provence
Giorgio Puggelli
Satya Pullela
Iksoo Pyo
Isa S. Qamber
Stefano Quer
Michael Quinn
Ivan Radivojevic
Richard Raimi
Rajesh Raina
Salil Raje
Suresh Rajgopal
Rajeev K. Ranjan
Sreenivasa Rao
Shishpal S. Rawat
Alain Raynaud
Bill Read
Maurizio Rebaudengo
Bob Reese
Michael Riepe
Andrew L. Rood
Wolfgang Rosenstiel
Charles Rosenthal
Roni Rosner
Rabindra K. Roy
Elizabeth Rudnick
P. Sadasivan
Hans Sahn
Alexander Saldanha
Yasunori Sameshima
Lejm Samir
Raul San Martin
Peter Sandborn
Sachin Sapatnekar
Majid Sarrafzadeh
Hidenori Sato
Koichi Sato
Janardhan H. Satyanarayana
Sunao Sawada
Prashant Sawkar
Riccardo Scarsi

Patrick R. Schaumont
Ulf Schlichtmann
Bernd Schuermann
Donatella Sciuto
Andrew Seawright
Carl Sechen
Joel Seidman
Masatoshi Sekine
Craig Selinger
Alexei Semenov
Jonjen Sern
Dorothy E. Setliff
Wen-Zen Shen
Narendra V. Shenoy
Will Sherwood
Hyongkyoon Shin
Thomas R. Shiple
Allan Silburt
L. Miguel Silveira
Eng J. Sin
Montek Singh
Vigyan Singhal
Mukund Sivaraman
Joseph P. Skudlarek
Eric Skuldt
Anna Slobodova
Mani Soma
Larry P. Soule
Lambert Spaanenburg
Rajagopala Srinivasan
Mysore Sriram
Brian Stacey
George Stamoulis
Balsha R. Stanisic
Don Stark
Jack A. Stinson
Leon Stok
Neal Stollon
Noel Strader
Ming Su
Peter R. Suaris
P.A. Subrahmanyam
Ashok Sudarsanam
Stephen Sugiyama
Wei-Kai Sun
Peter Sutton
William Swartz
Frank Szorc
Thomas G. Szymanski

Masayoshi M. Tachibana
Paul Tafertshofer
Hiromasa Takahashi
Thomas Tamisier
Yutaka Tamiya
Gerard Tarroux
Ricardo Telichevesky
Chin-Chi Teng
Ramesh C. Terumalla
Shashidhar Thakur
Michael Theobald
Thorsten Theobald
Tzu-Chieh Tien
Adwin H. Timmer
Vivek Tiwari
Steve Tjiang
Paul G. Tobin
Robert Todd
Masahiko Toyonaga
Tuan Anh Tran
Stephen Trimberger
J. Donald Trotter
Anne-Marie Trullemans-Anckaert
Chien-Chun Tsai
Chung-Wen Tsao
Yu-Wen Tsay
Chi-Ying Tsui
Raymond Y. Tsui
Maura Turolla
Jon G. Udell
Hasan F. Ugurdag
Yasuo Unekawa
Radha Vaidyanathan
Hirendu Vaishnav
Jan Van Der Steen
A.J. Van Genderen
Lukas P.P.P. Van Ginneken
Jef Van Meerbergen
Johan Van Praet
Peter Vanbekbergen
Jagadeesh Vasudevamurthy
Rajagop Venkatachalam
G. Venkatesh
Ingrid Verbauwhede
Wim Verhaegh
Serge Vernalde
Idalina J. Videira
Tiziano Villa
Ashok Vittal

Jakob Vlietstra
Zeroen P. Voeten
Ronald L. Wadsack
Michael Wahl
Duncan M. Walker
Peter A. Walker
Robert A. Walker
Elizabeth Walkup
David Wallace
Ching-Yi Wang
Duen-Jeng Wang
Huey-Yih Wang
Jimmy S. Wang
Yifeng Wang
Greg Ward
Yen-Cheng Wen
Jen-Pin Weng
Jesse Whittemore
Manfred Wiesel
Markus Willems
Anthony Wojcik
Yaron Wolfsthal
Allen C.H. Wu
Chang Wu
Ephrem Wu
Tsung-Yi Wu
Bernhard Wunder
Bernd Wurth
Jiabei Xiao
Jin Xu
Min Xu
Songjie Xu
Alexandre Yakovlev
Hakan Yalcin
Koichi Yamashita
Lawrence R. Yang
Hiroto Yasuura
Dah-Cherng Yuan
Frank Y. Yuan
Joel T. Yuen
Roberto Zafalon
Peter W. Zepter
Jian-Kun Zhao
Hai Zhou
Zheng Zhou
Jiab J. Zhu
Jianwen Zhu
Thomas Ziaja
Vojin Zivojnovic

OPENING KEYNOTE ADDRESS

Scott G. McNealy
President/Chairman of the Board/CEO
Sun Microsystems, Inc.
Mountain View, CA

Under the leadership of co-founder Scott McNealy, Sun Microsystems, Inc. has become one of America's fastest-growing companies, according to *Fortune* magazine. The 41-year-old chief executive leads "the most efficient company in the industry," writes *Business Week*.

Mr. McNealy serves as Chairman of the Board, President and CEO of Sun, the parent company of all Sun subsidiaries and operating companies. With more than \$6 billion in annual revenues, Sun Microsystems ranks 222 on the Fortune 500. The company is the world's leading provider of powerful UNIX[®] workstations, servers and related software. Java[™], its platform-independent programming language, provides a comprehensive solution to the challenge of programming for complex networks, including the Internet.

Mr. McNealy has become an industry spokesman for open computer systems and a chief proponent of client-server, peer computing. He serves as Co-vice Chairman for the security encryption and export controls committee of the Computer Systems Policy Project, a consortium of 13 of the largest U.S. computer companies that address public policy issues affecting the industry and the nation. He is also on the Board of Directors of the Santa Clara County Manufacturers Board.

Mr. McNealy was Vice President of Operations at Sun before his appointment to President in February 1984. Prior to Sun, he was Director of Operations at Onyx Systems, a manufacturer of microcomputer systems, and a member of FMC's corporate manufacturing staff. He also held various operations and sales positions at Rockwell International.

Mr. McNealy was awarded a degree in economics from Harvard University and an M.B.A. from Stanford University.

THURSDAY KEYNOTE ADDRESS

Michael A. Aymar
Vice-President/General Manager
Intel Corp.
Santa Clara, CA

A VISION OF THE FUTURE OF COMPUTING

The pace of technology advancement in computing continues to accelerate. Mr. Aymar will offer a glimpse into the future of EDA design environment. The continued evolution will provide new capabilities which are based on standards, innovation, value and choice. Technologies such as video, audio, imaging, animation and the internet provide the foundation. These capabilities will improve your productivity at work and on the road, and provide new entertainment experiences at home.

Michael Aymar is Vice President and General Manager of Intel Corp.'s Desktop Products Group.

Mr. Aymar, who joined Intel in 1976, has extensive experience in micro- and mini-computer systems. Prior to his current assignment, he held positions in system and software engineering, microprocessor marketing, VLSI design automation, and general management assignments in development systems and mobile personal computers. Before coming to Intel, Mr. Aymar was employed by Hewlett-Packard.

A graduate of Stanford University, Mr. Aymar received both his B.S. and M.S. degrees, cum laude, in electrical engineering in 1970.

Table of Contents

General Chair's Welcome	iii
Executive Committee	iv
Technical Program Committee	vi
1997 Best Paper Award	ix
ACSEE Undergraduate Scholarships	ix
35th Call for Papers	x
Design Automation Conference Scholarship Awards	xi
Meritorious Service Award	xi
Reviewers	xii
Opening Keynote Address— <i>Scott G. McNealy</i>	xvi
Thursday Keynote Address— <i>Michael A. Aymar</i>	xvii

Panel: An Executive View of the EDA Industry

Chair: A. Richard Newton

Organizer: Mike Murray

Panel Members: *Joseph Costello, Aart de Geus, William Herman, Gerald Hsu,*

Keith Lobo, Walden Rhines.....1

Session 1

Sequential Synthesis

Chair: Richard L. Rudell

Organizers: Fabio Somenzi, Sharad Malik

1.1	An Improved Algorithm for Minimum-Area Retiming	
	<i>Naresh Maheshwari, Sachin S. Sapatnekar</i>	2
1.2	Efficient Latch Optimization Using Exclusive Sets	
	<i>Ellen M. Sentovich, Horia Toma, Gérard Berry</i>	8
1.3	Sequence Compaction for Probabilistic Analysis of Finite-State Machines	
	<i>Diana Marculescu, Radu Marculescu, Massoud Pedram</i>	12
1.4	Synthesis of Speed-Independent Circuits from STG-unfolding Segment	
	<i>Alexei Semenov, Alexandre Yakovlev, Enric Pastor, Marco A. Peña, Jordi Cortadella</i>	16
1.5	Telescopic Units: Increasing the Average Throughput of Pipelined Designs by Adaptive Latency Control	
	<i>Luca Benini, Enrico Macii, Massimo Poncino</i>	22

Session 2

Interconnect Modeling

Chair: Lawrence T. Pileggi

Organizers: Andrew T. Yang, Jacob White

2.1	Zeros and Passivity of Arnoldi-Reduced-Order Models for Interconnect Networks	
	<i>Ibrahim M. Elfadel, David D. Ling</i>	28
2.2	Preservation of Passivity During RLC Network Reduction via Split Congruence Transformations	
	<i>Kevin J. Kerns, Andrew T. Yang</i>	34
2.3	Lumped Interconnect Models Via Gaussian Quadrature	
	<i>Keith Nabors, Tze-Ting Fang, Hung-Wen Chang, Kenneth S. Kundert, Jacob K. White</i>	40
2.4	Calculating Worst-Case Gate Delays Due to Dominant Capacitance Coupling	
	<i>Florentin Dartu, Lawrence T. Pileggi</i>	46

Session 3

Novel Techniques for Software Scheduling

Chair: Gaetano Borriello

Organizers: Rajesh K. Gupta, Luciano Lavagno

- 3.1 Schedule Validation for Embedded Reactive Real-Time Systems**
Felice Balarin, Alberto Sangiovanni-Vincentelli.....52
- 3.2 Incorporating Imprecise Computation into System-Level Design of Application-Specific Heterogeneous Multiprocessors**
Yosef G. Tirat-Gefen, Diogenes C. Silva, Alice C. Parker.....58
- 3.3 Data Memory Minimisation for Synchronous Data Flow Graphs Emulated on DSP-FPGA Targets**
Marleen Adé, Rudy Lauwereins, J. A. Peperstraete.....64
- 3.4 An Efficient Implementation of Reactivity for Modeling Hardware in the Scenic Design Environment**
Stan Liao, Steve Tjiang, Rajesh Gupta.....70

Session 4

- 4.1 Embedded Tutorial: Tools and Methodologies for Low Power Design**
Jerry Frenkil76
- Panel: Low-Power Design Tools: Where Is the Impact?**
Chair: Jan M. Rabaey
Organizer: Nanette Collins
Panel Members: Bill Bell, Jerry Frenkil, Vassilios Gerousis, Massoud Pedram,
Deo Singh, Jim Sproch82

Session 5

Simulation Techniques for Microprocessors

Chair: Haruyuki Tago

Organizers: Haruyuki Tago, Neil Weste

- 5.1 A C-Based RTL Design Verification Methodology for Complex Microprocessor**
Joon-Seo Yim, Yoon-Ho Hwang, Chang-Jae Park, Hoon Choi, Woo-Seung Yang, Hun-Seung Oh, In-Cheol Park, Chong-Min Kyung83
- 5.2 Hierarchical Random Simulation Approach for the Verification of S/390 CMOS Multiprocessors**
Jörg Walter, Jens Leenstra, Gerhard Döttling, Bernd Leppla, Hans-Jürgen Münster, Kevin Kark, Bruce Wile89
- 5.3 Efficient Testing of Clock Regenerator Circuits in Scan Designs**
Rajesh Raina, Robert Bailey, Charles Njinda, Robert Molyneaux, Charlie Beh95
- 5.4 A Real-Time RTL Engineering-Change Method Supporting On-Line Debugging for Logic-Emulation Applications**
Wen-Jong Fang, Allen C.-H. Wu, Ti-Yen Yen101

Session 6

Combinational Logic Synthesis

Chair: Hamid Savoj

Organizers: Andreas Kuehlmann, Massoud Pedram

- 6.1 A Graph-Based Synthesis Algorithm for AND/XOR Networks**
Yibin Ye, Kaushik Roy107
- 6.2 Optimizing Designs Containing Black Boxes**
Tai-Hung Liu, Khurram Sajid, Adnan Aziz, Vigyan Singhal113

6.3	Solving Covering Problems Using LPR-Based Lower Bounds <i>Stan Liao, Srinivas Devadas</i>	117
6.4	Exact Coloring of Real-Life Graphs is Easy <i>Olivier Coudert</i>	121

Session 7

Interconnect Parasitic Extraction

Chair: Andrew T. Yang

Organizers: Jacob White, Jason Cong

7.1	Hierarchical 2-D Field Solution for Capacitance Extraction for VLSI Interconnect Modeling <i>E. Aykut Dengi, Ronald A. Rohrer</i>	127
7.2	Bounds for BEM Capacitance Extraction <i>Michael W. Beattie, Lawrence T. Pileggi</i>	133
7.3	SPIE: Sparse Partial Inductance Extraction <i>Zhijiang He, Mustafa Celik, Lawrence T. Pileggi</i>	137
7.4	A Fast Method of Moments Solver for Efficient Parameter Extraction of MCMs <i>Sharad Kapur, Jinsong Zhao</i>	141

Session 8

Advances in Timing Analysis for Embedded Software

Chair: Wendell Baker, Hiroto Yasuura

Organizers: Rajesh K. Gupta, Luciano Lavagno

8.1	Embedded Tutorial: Static Timing Analysis of Embedded Software <i>Sharad Malik, Margaret Martonosi, Yau-Tsun Steven Li</i>	147
8.2	A Task-Level Hierarchical Memory Model for System Synthesis of Multiprocessors <i>Yanbing Li, Wayne Wolf</i>	153
8.3	Predicting Timing Behavior in Architectural Design Exploration of Real-Time Embedded Systems <i>Rajeshkumar Sambandam, Xiaobo (Sharon) Hu</i>	157

Session 9

Applications of Formal Verification

Chair: Andreas Kuehlmann

Organizers: Haruyuki Tago, Neil Weste

9.1	Formal Verification of a Superscalar Execution Unit <i>Kyle L. Nelson, Alok Jain, Randal E. Bryant</i>	161
9.2	Formal Verification of Content Addressable Memories Using Symbolic Trajectory Evaluation <i>Manish Pandey, Richard Raimi, Randal E. Bryant, Magdy S. Abadir</i>	167
9.3	Formal Verification of FIRE: A Case Study <i>Jae-Young Jang, Shaz Qadeer, Matt Kaufmann, Carl Pixley</i>	173

Session 10

System-Level Exploration and Refinement

Chair: Ivo Bolsens

Organizers: Ivo Bolsens, Anders Forsen

10.1	Interface-Based Design <i>James A. Rowson, Alberto Sangiovanni-Vincentelli</i>	178
10.2	An Integrated Design Environment for Performance and Dependability Analysis <i>Robert H. Klenke, Moshe Meyassed, James H. Aylor, Barry W. Johnson, Ramesh Rao, Anup Ghosh</i>	184

10.3	A Dynamic Design Estimation and Exploration Environment <i>Ole Bentz, Jan M. Rabaey, David B. Lidsky</i>190
------	---

Session 11

Binary Decision Diagrams

Chair: Andreas Kuehlmann

Organizers: Massoud Pedram, Andreas Kuehlmann

11.1	Remembrance of Things Past: Locality and Memory in BDDs <i>Srilatha Manne, Dirk Grunwald, Fabio Somenzi</i>196
11.2	Linear Sifting of Decision Diagrams <i>Christoph Meinel, Fabio Somenzi, Thorsten Theobald</i>202
11.3	Safe BDD Minimization Using Don't Cares <i>Youpyo Hong, Peter A. Beerel, Jerry R. Burch, Kenneth L. McMillan</i>208

Session 12

Timing Analysis

Chair: Karem A. Sakallah

Organizers: Karem Sakallah, Sharad Malik

12.1	Timing Optimization for Multi-Source Nets: Characterization and Optimal Repeater Insertion <i>John Lillis, Chung-Kuan Cheng</i>214
12.2	Exact Required Time Analysis via False Path Detection <i>Yuji Kukimoto, Robert K. Brayton</i>220
12.3	Symbolic Timing Verification of Timing Diagrams using Presburger Formulas <i>Tod Amon, Gaetano Borriello, Taokuan Hu, Jiwen Liu</i>226

Session 13

Embedded Tutorial: Code Generation for Core Processors

13.1	Chair: Peter Marwedel Organizers: Giovanni De Micheli Presenter: <i>Peter Marwedel</i>232
------	---

Session 14

Panel: Physical Design and Synthesis: Merge or Die!

Chair: Massoud Pedram

Organizer: Massoud Pedram

Panel Members: *Richard Bushroo, Raul Camposano, Giovanni De Micheli, Antun Domic,*

Chi-Ping Hsu, Michael Jackson238

Session 15

System-Level Optimization and Verification

Chair: Phil Duncan

Organizers: Ivo Bolsens, James A. Rowsen

15.1	Interface Timing Verification Drives System Design <i>Ajay J. Daga, Peter R. Suaris</i>240
15.2	Memory-CPU Size Optimization for Embedded System Designs <i>Barry Shackelford, Mitsuhiro Yasuda, Etsuko Okushi, Hisao Koizumi, Hiroyuki Tomiyama, Hiroto Yasuura</i>246
15.3	Methodology for Behavioral Synthesis-based Algorithm-level Design Space Exploration: DCT Case Study <i>Miodrag Potkonjak, Kyosun Kim, Ramesh Karri</i>252

Session 16

Formal Verification

Chair: Fabio Somenzi

Organizers: Fabio Somenzi, Giovanni De Micheli

16.1	Embedded Tutorial: Formal Verification in a Commercial Setting <i>R. P. Kurshan</i>	258
16.2	Equivalence Checking Using Cuts and Heaps <i>Andreas Kuehlmann, Florian Krohm</i>	263

Session 17

Analog Simulation

Chair: Giorgio Casinovi

Organizers: Jacob White, Hidetoshi Onodera

17.1	Efficient Methods for Simulating Highly Nonlinear Multi-Rate Circuits <i>Jaijeet Roychowdhury</i>	269
17.2	Rapid Frequency-Domain Analog Fault Simulation Under Parameter Tolerances <i>Michael W. Tian, C.-J. Richard Shi</i>	275
17.3	SWITTEST: Automatic Switch-level Fault Simulation and Test Evaluation of Switched-Capacitor Systems <i>S. Mir, A. Rueda, T. Olbrich, E. Peralías, J. L. Huertas</i>	281

Session 18

Software Synthesis for Embedded Systems

Chair: Sharad Malik

Organizers: Sharad Malik, Luciano Lavagno

18.1	Analysis and Evaluation of Address Arithmetic Capabilities in Custom DSP Architectures <i>Ashok Sudarsanam, Stan Liao, Srinivas Devadas</i>	287
18.2	System Level Fixed-Point Design Based on an Interpolative Approach <i>Markus Willems, Volker Bürgens, Holger Keding, Thorsten Grötter, Heinrich Meyr</i>	293
18.3	ISDL: An Instruction Set Description Language for Retargetability <i>George Hadjiyiannis, Silvina Hanono, Srinivas Devadas</i>	299
18.4	Generation of Software Tools from Processor Descriptions for Hardware/Software Codesign <i>Mark R. Hartoog, James A. Rowson, Prakash D. Reddy, Soumya Desai, Douglas D. Dunlop, Edwin A. Harcourt, Neeti Khullar</i>	303

Session 19

Experiences in System Design and Education at Universities

Chairs: Jan M. Rabaey, Anantha Chandrakasan

Organizers: Jan M. Rabaey

19.1	Education for the Deep-Submicron Age: Business As Usual? <i>Hugo De Man</i>	307
19.2	INFOPAD: An Experiment in System-Level Design and Integration <i>Robert W. Brodersen</i>	313
19.3	Very Rapid Prototyping of Wearable Computers: A Case Study of Custom Versus Off-the-Shelf Design Methodologies <i>Asim Smailagic, Daniel P. Siewiorek, Richard Martin, John Stivoric</i>	315

Session 20

Standard Cell and Physical Design Methods

Chair: Neil Weste

Organizers: Neil Weste, Randolph E. Harr

20.1	CAD at the Design-Manufacturing Interface <i>H. T. Heineken, J. Khare, W. Maly, P. K. Nag, C. Ouyang, W. A. Pleskacz</i>	321
20.2	CELLERITY: A Fully Automatic Layout Synthesis System for Standard Cell Libraries <i>Mohan Guruswamy, Robert L. Maziasz, Daniel Dulitz, Srilata Raman, Venkat Chiluvuri, Andrea Fernandez, Larry G. Jones</i>	327
20.3	Developing a Concurrent Methodology for Standard-Cell Library Generation <i>Donald G. Baltus, Thomas Varga, Robert C. Armstrong, John Duh, T. G. Matheson</i>	333
20.4	A Fast and Accurate Technique to Optimize Characterization Tables for Logic Synthesis <i>John F. Croix, Martin D. F. Wong</i>	337

Session 21

Modeling and Transformations in Synthesis

Chair: David Ku

Organizers: Kazutoshi Wakabayashi, Raul Camposano

21.1	Limited Exception Modeling and Its Use in Presynthesis Optimization <i>Jian Li, Rajesh K. Gupta</i>	341
21.2	Potential-Driven Statistical Ordering of Transformations <i>Inki Hong, Darko Kirovski, Miodrag Potkonjak</i>	347
21.3	Synthesis of Application Specific Programmable Processors <i>Kyosun Kim, Ramesh Karri, Miodrag Potkonjak</i>	353
21.4	Symbolic Evaluation of Performance Models for Tradeoff Visualization <i>Jeffrey Walrath, Ranga Vemuri</i>	359

Session 22

Statistical Power Estimation Techniques

Chair: Luca Benini

Organizers: Massoud Pedram, Andrew T. Yang

22.1	Power Macromodeling for High Level Power Estimation <i>Subodh Gupta, Farid N. Najm</i>	365
22.2	Statistical Estimation of the Cumulative Distribution Function for Power Dissipation in VLSI Circuits <i>Chih-Shun Ding, Qing Wu, Cheng-Ta Hsieh, Massoud Pedram</i>	371
22.3	Statistical Estimation of Average Power Dissipation in Sequential Circuits <i>Li-Pen Yuan, Chin-Chi Teng, Sung-Mo Kang</i>	377
22.4	Vector Generation for Maximum Instantaneous Current Through Supply Lines for CMOS Circuits <i>Angela Krstić, Kwang-Ting (Tim) Cheng</i>	383

Session 23

Co-Simulation

Chair: Kunle Olukotun

Organizers: Rajesh Gupta, Kunle Olukoton

23.1	Fast Hardware/Software Co-Simulation for Virtual Prototyping and Trade-Off Analysis <i>Claudio Passerone, Luciano Lavagno, Massimiliano Chiodo, Alberto Sangiovanni-Vincentelli</i>	389
23.2	Dynamic Communication Models in Embedded System Co-Simulation <i>Ken Hines, Gaetano Borriello</i>	395

Session 24

Panel: Challenges in Worldwide IP Reuse

Chair: Rita Glover

Organizers: Takahide Inoue, Rita Glover, John Teets

Panel Members: Doug Fairbairn, Larry Cooke, Steve Schulz, Takahide Inoue,

Raj Raghavan, Jean-Louis Bories, Wally Rhines401

Session 25

Emerging Technologies and Architectures for Low Power

Chair: Vivek Tiwari

Organizers: Anatha Chandrakasan, Robert C. Frye

25.1	Device-Circuit Optimization for Minimal Energy and Power Consumption in CMOS Random Logic Networks <i>Pankaj Pant, Vivek De, Abhijit Chatterjee</i>403
25.2	Transistor Sizing Issues and Tool for Multi-Threshold CMOS Technology <i>James Kao, Anantha Chandrakasan, Dimitri Antoniadis</i>409
25.3	Architectural Exploration Using Verilog-Based Power Estimation: A Case Study of the IDCT <i>Thucydides Xanthopoulos, Yoshifumi Yaoi, Anantha Chandrakasan</i>415
25.4	A Power Estimation Framework for Designing Low Power Portable Video Applications <i>Chi-Ying Tsui, Kai-Keung Chan, Qing Wu, Chih-Shun Ding, Massoud Pedram</i>421
25.5	An Investigation of Power Delay Trade-Offs on PowerPC Circuits <i>Qi Wang, Sarma B. K. Vrudhula, Shantanu Ganguly</i>425

Session 26

High Level Synthesis for Low Power

Chair: Kazutoshi Wakabayashi

Organizers: Raul Camposano, Kazutoshi Wakabayashi

26.1	Power Management Techniques for Control-Flow Intensive Designs <i>Anand Raghunathan, Sujit Dey, Niraj K. Jha, Kazutoshi Wakabayashi</i>429
26.2	Low Energy Memory and Register Allocation Using Network Flow <i>Catherine H. Gebotys</i>435
26.3	Power-Conscious High Level Synthesis Using Loop Folding <i>Daehong Kim, Kiyoun Choi</i>441

Session 27

Module Generation

Chair: Dwight D. Hill

Organizers: Antun Domic, Patrick Groeneveld

27.1	Embedded Tutorial: The Future of Custom Cell Generation in Physical Synthesis <i>Martin Lefebvre, David Marple, Carl Sechen</i>446
27.2	CLIP: An Optimizing Layout Generator for Two-Dimensional CMOS Cells <i>Avaneendra Gupta, John P. Hayes</i>452
27.3	An Efficient Transistor Folding Algorithm for Row-Based CMOS Layout Design <i>Jaewon Kim, S. M. Kang</i>456
27.4	Technology Retargeting for IC Layout <i>John Lakos</i>460

Session 28

BIST and DFT

Chair: Yervant Zorian

Organizers: Janusz Rajski, Yervant Zorian

28.1	A Test Synthesis Approach to Reducing BALLAST DFT Overhead <i>Douglas Chang, Mike Tien-Chien Lee, Malgorzata Marek-Sadowska, Takashi Aikyo, Kwang-Ting Cheng</i>	466
28.2	STARBIST: Scan Autocorrelated Random Pattern Generation <i>K. H. Tsai, S. Hellebrand, J. Rajski, M. Marek-Sadowska</i>	472
28.3	A Hybrid Algorithm for Test Point Selection for Scan-Based BIST <i>Huan-Chih Tsai, Kwang-Ting Cheng, Chih-Jen Lin, Sudipta Bhawmik</i>	478

Session 29

Panel: Hardware/Software Co-Verification

Chair: Gary Smith

Organizers: Michel Courtoy, Marion Kenefick

Panel Members: *Brian Bailey, Kurt Keutzer, Amr Mohsen, Richard Moseley, Jim Rowson, Geoff Bunza, Willis Hendley*.....484

Session 30

DSP & Telecommunication System Design

Chair: Rajeev Jain

Organizers: Phil Duncan, Teresa Meng

30.1	Design and Synthesis of Array Structured Telecommunication Processing Applications <i>Wolfgang Meyer, Andrew Seawright, Fumiya Tada</i>	486
30.2	RASSP Virtual Prototyping of DSP Systems <i>C. Hein, J. Pridgen, W. Kline</i>	492
30.3	A Parallel/Serial Trade-Off Methodology for Look-Up Table Based Decoders <i>Claus Schneider</i>	498

Session 31

Embedded Tutorial: High Level Power Modeling, Estimation, and Optimization

31.1	Chair: Massoud Pedram Organizers: Giovanni De Micheli, Massoud Pedram Presenters: <i>Enrico Macii, Massoud Pedram, Fabio Somenzi</i>	504
------	--	-----

Session 32

Advances in Partitioning

Chair: Martin D. F. Wong

Organizers: Antun Domic, Patrick Groeneveld

32.1	A Network Flow Approach for Hierarchical Tree Partitioning <i>Ming-Ter Kuo, Chung-Kuan Cheng</i>	512
32.2	Multi-Way FPGA Partitioning by Fully Exploiting Design Hierarchy <i>Wen-Jong Fang, Allen C.-H. Wu</i>	518
32.3	A Hierarchy-Driven FPGA Partitioning Method <i>Helena Krupnova, Ali Abbata, Gabrièle Saucier</i>	522
32.4	Multilevel Hypergraph Partitioning: Application in VLSI Domain <i>George Karypis, Rajat Aggarwal, Vipin Kumar, Shashi Shekhar</i>	526
32.5	Multilevel Circuit Partitioning <i>Charles J. Alpert, Jen-Hsin Huang, Andrew B. Kahng</i>	530

Session 33

Processor Test Techniques

Chair: Janusz Rajski

Organizers: Yervant Zorian, Janusz Rajski

33.1	Hierarchical Test Generation and Design for Testability of ASPPs and ASIPs <i>Indradeep Ghosh, Anand Raghunathan, Niraj K. Jha</i>	534
33.2	Frequency-Domain Compatibility in Digital Filter BIST <i>Laurence Goodby, Alex Orailoglu</i>	540
33.3	A Scheme for Integrated Controller-Datapath Fault Testing <i>M. Nourani, J. Carletta, C. Papachristou</i>	546

Session 34

Panel: The Next Generation HDL

Chair: Steve E. Schulz

Organizers: Richard Goering, Nanette Collins

Panel Members: Gerard Berry, Kurt Keutzer, Maq Mannan, James A. Rowson,
Alberto Sangiovanni-Vincentelli, Larry Saunders.....552

Session 35

Design Processes and Frameworks

Chair: Teresa Meng

Organizers: Teresa Meng, Jan M. Rabaey

35.1	Executable Workflows: A Paradigm for Collaborative Design on the Internet <i>Hemang Lavana, Amit Khetawat, Franc Brglez, Krzysztof Kozminski</i>	553
35.2	Electronic Component Information Exchange (ECIX) <i>Donald R. Cottrell</i>	559
35.3	Modeling Design Tasks and Tools - The Link Between Product and Flow Model <i>Bernd Schürmann, Joachim Altmeyer</i>	564

Session 36

Probabilistic Models of Input Data for Efficient Power Estimation

Chair: Farid N. Najm

Organizers: Fabio Somenzi, Andrew T. Yang

36.1	Hierarchical Sequence Compaction for Power Estimation <i>Radu Marculescu, Diana Marculescu, Massoud Pedram</i>	570
36.2	Profile-Driven Program Synthesis for Evaluation of System Power Dissipation <i>Cheng-Ta Hsieh, Massoud Pedram, Gaurav Mehta, Fred Rastgar</i>	576
36.3	Analytical Estimation of Transition Activity from Word-Level Signal Statistics <i>Sumant Ramprasad, Naresh R. Shanbhag, Ibrahim N. Hajj</i>	582

Session 37

Hot Topics in Routing

Chair: Carl Sechen

Organizers: Patrick Groeneveld, Antun Domic

37.1	Wire Segmenting for Improved Buffer Insertion <i>Charles Alpert, Anirudh Devgan</i>	588
37.2	More Practical Bounded-Skew Clock Routing <i>Andrew B. Kahng, C.-W. Albert Tsao</i>	594
37.3	An Efficient Approach to Multi-Layer Layer Assignment with Application to Via Minimization <i>Chin-Chih Chang, Jason Cong</i>	600

37.4	Optimal Wire-Sizing Function with Fringing Capacitance Consideration <i>Chung-Ping Chen, D. F. Wong</i>	604
------	---	-----

Session 38

Test Generation and Fault Simulation

Chair: Vishwani Agrawal

Organizers: Yervant Zorian, Janusz Rajski

38.1	Fault Simulation Under the Multiple Observation Time Approach Using Backward Implications <i>Irith Pomeranz, Sudhakar M. Reddy</i>	608
38.2	ATPG for Heat Dissipation Minimization during Scan Testing <i>Seongmoon Wang, Sandeep K. Gupta</i>	614
38.3	Automatic Generation of Synchronous Test Patterns for Asynchronous Circuits <i>Oriol Roig, Jordi Cortadella, Marco A. Peña, Enric Pastor</i>	620

Session 39

Panel: The Road Ahead in CPLD & FPGA Design Methodology

Chair: Rhondalee Rohleder

Organizer: John Birkner

Panel Members: *Don Faria, Steve Golson, Robert K. Beachler, Bruce Kleinman,*

Mike Dini, Bob Donaldson, Dave Kohlmeier.....

626

Session 40

Deep Submicron Modeling and Analysis

Chair: Robert C. Frye

Organizers: Vivek Tiwari, Anantha Chandrakasan

40.1	Analysis and Justification of a Simple, Practical 2 1/2-D Capacitance Extraction Methodology <i>Jason Cong, Lei He, Andrew B. Kahng, David Noice, Nagesh Shirali, Steven H.-C. Yen</i>	627
40.2	Accurate and Efficient Macromodel of Submicron Digital Standard Cells <i>Cristiano Forzan, Bruno Franzini, Carlo Guardiani</i>	633
40.3	Power Supply Noise Analysis Methodology for Deep-Submicron VLSI Chip Design <i>Howard H. Chen, David D. Ling</i>	638

Session 41

Technology-Dependent Optimization for Performance and Power

Chair: Gabriele Saucier

Organizers: Jason Cong, Gabriele Saucier

41.1	FPGA Synthesis with Retiming and Pipelining for Clock Period Minimization of Sequential Circuits <i>Jason Cong, Chang Wu</i>	644
41.2	Technology-Dependent Transformations for Low-Power Synthesis <i>Rajendran Panda, Farid N. Najm</i>	650
41.3	Low Power FPGA Design - A Re-engineering Approach <i>Chau-Shen Chen, TingTing Hwang, C.L. Liu</i>	656
41.4	Post-Layout Logic Restructuring for Performance Optimization <i>Yi-Min Jiang, Angela Krstic, Kwang-Ting Cheng, Malgorzata Marek-Sadowska</i>	662
41.5	Layout Driven Re-Synthesis for Low Power Consumption LSIs <i>Masako Murofushi, Takashi Ishioka, Masami Murakata, Takashi Mitsuhashi</i>	666

Session 42

CAD Issues for Micro-Electro-Mechanical Systems

Chair: Randolph E. Harr

Organizers: Randolph E. Harr, Jacob White

42.1	Embedded Tutorial: Overview of Microelectromechanical Systems and Design Processes	
	<i>William C. Tang</i>	670
42.2	CAD and Foundries for Microsystems	
	<i>J. M. Karam, B. Courtois, H. Boutamine, P. Drake, A. Poppe, V. Szekely, M. Rencz, K. Hofmann, M. Glesner</i>	674
42.3	Structured Design of Microelectromechanical Systems	
	<i>Tamal Mukherjee, Gary K. Fedder</i>	680
42.4	Algorithms for Coupled Domain MEMS Simulation	
	<i>N. Aluru, J. White</i>	686

Session 43

Hardware/Software Partitioning

Chair: Rolf Ernst

Organizers: Luciano Lavagno, Rajesh K. Gupta

43.1	A Hardware/Software Partitioner Using a Dynamically Determined Granularity	
	<i>Jörg Henkel, Rolf Ernst</i>	691
43.2	System-Level Synthesis of Low-Power Hard Real-Time Systems	
	<i>Darko Kirovski, Miodrag Potkonjak</i>	697
43.3	COSYN: Hardware-Software Co-Synthesis of Embedded Systems	
	<i>Bharat P. Dave, Ganesh Lakshminarayana, Niraj K. Jha</i>	703
43.4	Data-Flow Assisted Behavioral Partitioning for Embedded Systems	
	<i>Samir Agrawal, Rajesh K. Gupta</i>	709
43.5	Hardware/Software Partitioning and Pipelining	
	<i>Smita Bakshi, Daniel D. Gajski</i>	713

Session 44

44.1	Embedded Tutorial: Chip Parasitic Extraction and Signal Integrity Verification	
	<i>Wayne W.-M. Dai</i>	717

Panel: Noise and Signal Integrity in Deep Submicron Design

Chair: William E. Guthrie

Organizer: Massoud Pedram

Panel Members: Rakesh Chadha, Jason Cong, Charlie Xiaoli Huang, Anirudh Devgan,

Tom Mozdzen, Andrew Yang

Session 45

Designing High Performance and Low Power Microprocessors Using Full Custom Techniques

Chair: Anantha Chandrakasan

Organizer: Anantha Chandrakasan

45.1	Designing High Performance CMOS Microprocessors Using Full Custom Techniques	
	<i>William J. Grundmann, Dan Dobberpuhl, Randy L. Allmon, Nicholas L. Rethman</i>	722

Session 46

Formal Verification Techniques

Chair: Rich Goldman

Organizers: Andreas Kuehlmann, Fabio Somenzi

46.1	Disjunctive Partitioning and Partial Iterative Squaring: An Effective Approach for Symbolic Traversal of Large Circuits <i>Gianpiero Cabodi, Paolo Camurati, Luciano Lavagno, Stefano Quer</i>728
46.2	An Efficient Assertion Checker for Combinational Properties <i>Gagan Hasteer, Anmol Mathur, Prithviraj Banerjee</i>734
46.3	Toward Formalizing a Validation Methodology Using Simulation Coverage <i>Aarti Gupta, Sharad Malik, Pranav Ashar</i>740

Session 47

Placement Techniques

Chair: Malgorzata Marek-Sadowska

Organizers: Patrick Groeneveld, Antun Domic

47.1	Algorithms for Large-Scale Flat Placement <i>Jens Vygen</i>746
47.2	Quadratic Placement Revisited <i>C. J. Alpert, T. Chan, D. J.-H. Huang, I. Markov, K. Yan</i>752
47.3	Unification of Budgeting and Placement <i>Majid Sarrafzadeh, David Knol, Gustavo Tellez</i>758
47.4	Cluster Refinement for Block Placement <i>Jin Xu, Pei-Ning Guo, Chung-Kuan Cheng</i>762

Session 48

Panel: The EDA Startup Experience: Financing the Venture

Chair: A. K. Kalekos

Organizer: Mike Murray

Panel Members: Marty Walker, Penny Herscher, Lucio Lanza, Peter Odrina,

John Cooper, Gerrald Langelier.....766

Session 49

Heterogeneous System Analysis

Chairs: Randolph E. Harr, Richard Smith

Organizers: David Blaauw, Jan M. Rabaey

49.1	Computer-Aided Design of Free-Space Opto-Electronic Systems <i>S. P. Levitan, P. J. Marchand, T. P. Kurzweg, M. A. Rempel, D. M. Chiarulli, C. Fan, F. B. McCormick</i>768
49.2	Hardware/Software Co-Simulation in a VHDL-Based Test Bench Approach <i>Matthias Bauer, Wolfgang Ecker</i>774
49.3	An Embedded System Case Study: The FirmWare Development Environment for a Multimedia Audio Processor <i>Clifford Liem, Marco Cornero, Miguel Santana, Pierre Paulin, Ahmed Jerraya, Jean-Marc Gentit, Jean Lopez, Xavier Figari, Laurent Bergher</i>780

Conference Author/Panelist Index

A

Abadir, M. S. 167
 Abbara, A. 522
 Adé, M. 64
 Aggarwal, R. 526
 Agrawal, S. 709
 Aikyo, T. 466
 Allmon, R. L. 722
 Alpert, C. 588
 Alpert, C. J. 530, 752
 Altmeyer, J. 564
 Aluru, N. 686
 Amon, T. 226
 Antoniadis, D. 409
 Armstrong, R. C. 333
 Ashar, P. 740
 Aylor, J. H. 184
 Aziz, A. 113

B

Bailey, B. 484
 Bailey, R. 95
 Bakshi, S. 713
 Balarin, F. 52
 Baltus, D. G. 333
 Banerjee, P. 734
 Bauer, M. 774
 Beachler, R. K. 626
 Beattie, M. W. 133
 Beerel, P. A. 208
 Beh, C. 95
 Bell, B. 82
 Benini, L. 22
 Bentz, O. 190
 Bergher, L. 780
 Berry, G. 8, 552
 Bhawmik, S. 478
 Bories, J.-L. 401
 Borriello, G. 226, 395
 Boutamine, H. 674
 Brayton, R. K. 220
 Brglez, F. 553
 Brodersen, R. W. 313
 Bryant, R. E. 161, 167
 Bunza, G. 484
 Burch, J. R. 208
 Bürgens, V. 293
 Bushroe, R. 238

C

Cabodi, G. 728
 Camposano, R. 238
 Camurati, P. 728
 Carletta, J. 546
 Celik, M. 137
 Chadha, R. 720
 Chan, K.-K. 421
 Chan, T. 752
 Chandrakasan, A. 409, 415
 Chang, C.-C. 600

Chang, D. 466
 Chang, H.-W. 40
 Chatterjee, A. 403
 Chen, C.-P. 604
 Chen, C.-S. 656
 Chen, H. H. 638
 Cheng, C.-K. 214, 512, 762
 Cheng, K.-T. 383, 466, 478, 662
 Chiarulli, D. M. 768
 Chiluvuri, V. 327
 Chiodo, M. 389
 Choi, H. 83
 Choi, K. 441
 Cong, J. 600, 627, 644, 720
 Cooke, L. 401
 Cooper, J. 766
 Cornero, M. 780
 Cortadella, J. 16, 620
 Costello, J. 1
 Cottrell, D. R. 559
 Coudert, O. 121
 Courtois, B. 674
 Croix, J. F. 337

D

Daga, A. J. 240
 Dai, W. W.-M. 717
 Dartu, F. 46
 Dave, B. P. 703
 De, V. 403
 de Geus, A. 1
 De Man, H. 307
 De Micheli, G. 238
 Dengi, E. A. 127
 Desai, S. 303
 Devadas, S. 117, 287, 299
 Devgan, A. 588, 720
 Dey, S. 429
 Ding, C.-S. 371, 421
 Dini, M. 626
 Dobberpuhl, D. 722
 Domic, A. 238
 Donaldson, B. 626
 Döttling, G. 89
 Drake, P. 674
 Duh, J. 333
 Dulitz, D. 327
 Dunlop, D. D. 303

E

Ecker, W. 774
 Elfadel, I. M. 28
 Ernst, R. 691

F

Fairbairn, D. 401
 Fan, C. 768
 Fang, T.-T. 40
 Fang, W.-J. 101, 518

Faria, D. 626
 Fedder, G. K. 680
 Fernandez, A. 327
 Figari, X. 780
 Forzan, C. 633
 Franzini, B. 633
 Frenkil, J. 76, 82

G

Gajski, D. D. 713
 Ganguly, S. 425
 Gebotys, C. H. 435
 Gentit, J.-M. 780
 Gerousis, V. 82
 Ghosh, A. 184
 Ghosh, I. 534
 Glesner, M. 674
 Golson, S. 626
 Goodby, L. 540
 Grötter, T. 293
 Grundmann, W. J. 722
 Grunwald, D. 196
 Guardiani, C. 633
 Guo, P.-N. 762
 Gupta, A. 452, 740
 Gupta, R. 70
 Gupta, R. K. 341, 709
 Gupta, S. 365
 Gupta, S. K. 614
 Guruswamy, M. 327

H

Hadjiyiannis, G. 299
 Hajj, I. N. 582
 Hanono, S. 299
 Harcourt, E. A. 303
 Hartoog, M. R. 303
 Hasteer, G. 734
 Hayes, J. P. 452
 He, L. 627
 He, Z. 137
 Hein, C. 492
 Heineken, H. T. 321
 Hellebrand, S. 472
 Hendley, W. 484
 Henkel, J. 691
 Herman, W. 1
 Herscher, P. 766
 Hines, K. 395
 Hofmann, K. 674
 Hong, I. 347
 Hong, Y. 208
 Hsieh, C.-T. 371, 576
 Hsu, C.-P. 238
 Hsu, G. 1
 Hu, T. 226
 Hu, X. 157
 Huang, C. X. 720
 Huang, D. J.-H. 752
 Huang, J.-H. 530

Huertas, J. L. 281
Hwang, T. 656
Hwang, Y.-H. 83

I

Inoue, T. 401
Ishioka, T. 666

J

Jackson, M. 238
Jain, A. 161
Jang, J.-Y. 173
Jerraya, A. 780
Jha, N. K. 429, 534, 703
Jiang, Y.-M. 662
Johnson, B. W. 184
Jones, L. G. 327

K

Kahng, A. B. 530, 594, 627
Kang, S. M. 377, 456
Kao, J. 409
Kapur, S. 141
Karam, J. M. 674
Kark, K. 89
Karri, R. 252, 353
Karypis, G. 526
Kaufmann, M. 173
Keding, H. 293
Kerns, K. J. 34
Keutzer, K. 484, 552
Khare, J. 321
Khetawat, A. 553
Khullar, N. 303
Kim, D. 441
Kim, J. 456
Kim, K. 252, 353
Kirovski, D. 347, 697
Kleinman, B. 626
Klenke, R. H. 184
Kline, W. 492
Knol, D. 758
Kohlmeier, D. 626
Koizumi, H. 246
Kozminski, K. 553
Krohm, F. 263
Krstic, A. 383, 662
Krupnova, H. 522
Kuehlmann, A. 263
Kukimoto, Y. 220
Kumar, V. 526
Kundert, K. S. 40
Kuo, M.-T. 512
Kurshan, R. P. 258
Kurzweg, T. P. 768
Kyung, C.-M. 83

L

Lakos, J. 460
Lakshminarayana, G. 703
Langelier, G. 766
Lanza, L. 766
Lauwereins, R. 64
Lavagno, L. 389, 728

Lavana, H. 553
Lee, M. T.-C. 466
Leenstra, J. 89
Lefebvre, M. 446
Leppla, B. 89
Levitani, S. P. 768
Li, J. 341
Li, S. 147
Li, Y. 153
Liao, S. 70, 117, 287
Lidsky, D. B. 190
Liem, C. 780
Lillis, J. 214
Lin, C.-J. 478
Ling, D. D. 28, 638
Liu, C. L. 656
Liu, J. 226
Liu, T.-H. 113
Lobo, K. 1
Lopez, J. 780

M

Macii, E. 22, 504
Maheshwari, N. 2
Malik, S. 147, 740
Maly, W. 321
Mannan, M. 552
Manne, S. 196
Marchand, P. J. 768
Marculescu, D. 12, 570
Marculescu, R. 12, 570
Marek-Sadowska, M. 466, 472, 662
Markov, I. 752
Marple, D. 446
Martin, R. 315
Martonosi, M. 147
Marwedel, P. 232
Matheson, T. G. 333
Mathur, A. 734
Maziasz, R. L. 327
McCormick, F. B. 768
McMillan, K. L. 208
Mehta, G. 576
Meinel, C. 202
Meyassed, M. 184
Meyer, W. 486
Meyr, H. 293
Mir, S. 281
Mitsuhashi, T. 666
Mohsen, A. 484
Molyneaux, R. 95
Moseley, R. 484
Mozdzen, T. 720
Mukherjee, T. 680
Münster, H.-J. 89
Murakata, M. 666
Murofushi, M. 666

N

Nabors, K. 40
Nag, P. K. 321
Najm, F. N. 365, 650
Nelson, K. L. 161
Njinda, C. 95
Noice, D. 627
Nourani, M. 546

O

Odrina, P. 766
Oh, H.-S. 83
Okushi, E. 246
Olbrich, T. 281
Orailoglu, A. 540
Ouyang, C. 321

P

Panda, R. 650
Pandey, M. 167
Pant, P. 403
Papachristou, C. 546
Park, C.-J. 83
Park, I.-C. 83
Parker, A. C. 58
Passerone, C. 389
Pastor, E. 16, 620
Paulin, P. 780
Pedram, M. 12, 82, 371, 421, 504, 570, 576
Peña, M. A. 16, 620
Peperstraete, J. A. 64
Peralías, E. 281
Pileggi, L. T. 46, 133, 137
Pixley, C. 173
Pleskacz, W. A. 321
Pomeranz, I. 608
Poncino, M. 22
Poppe, A. 674
Potkonjak, M. 252, 347, 353, 697
Pridgen, J. 492

Q

Qadeer, S. 173
Quer, S. 728

R

Rabaey, J. M. 190
Raghavan, R. 401
Raghunathan, A. 429, 534
Raimi, R. 167
Raina, R. 95
Rajski, J. 472
Raman, S. 327
Ramprasad, S. 582
Rao, R. 184
Rastgar, F. 576
Reddy, P. D. 303
Reddy, S. M. 608
Rempel, M. A. 768
Rencz, M. 674
Rethman, N. L. 722
Rhines, W. 1, 401
Rohrer, R. A. 127
Roig, O. 620
Rowson, J. 484
Rowson, J. A. 178, 303, 552
Roy, K. 107
Roychowdhury, J. 269
Rueda, A. 281

S

Sajid, K. 113
Sambandam, R. 157
Sangiovanni-Vincentelli, A. 52, 178, 389, 552
Santana, M. 780
Sapatnekar, S. S. 2
Sarrafzadeh, M. 758
Saucier, G. 522
Saunders, L. 552
Schneider, C. 498
Schulz, S. 401
Schürmann, B. 564
Seawright, A. 486
Sechen, C. 446
Semenov, A. 16
Sentovich, E. M. 8
Shackleford, B. 246
Shanbhag, N. R. 582
Shekhar, S. 526
Shi, C.-J. R. 275
Shirali, N. 627
Siewiorek, D. P. 315
Silva, D. C. 58
Singh, D. 82
Singhal, V. 113
Smailagic, A. 315
Somenzi, F. 196, 202, 504
Sproch, J. 82
Stivoric, J. 315
Suaris, P. R. 240
Sudarsanam, A. 287
Szekely, V. 674

T

Tada, F. 486
Tang, W. C. 670
Tellez, G. 758
Teng, C.-C. 377
Theobald, T. 202
Tian, M. W. 275
Tirat-Gefen, Y. G. 58
Tjiang, S. 70
Toma, H. 8
Tomiyama, H. 246
Tsai, H.-C. 478
Tsai, K. H. 472
Tsao, C.-W. A. 594
Tsui, C.-Y. 421

V

Varga, T. 333
Vemuri, R. 359
Vrudhula, S. B. K. 425
Vygen, J. 746

W

Wakabayashi, K. 429
Walker, M. 766
Walrath, J. 359
Walter, J. 89
Wang, Q. 425
Wang, S. 614
White, J. 686
White, J. K. 40

Wile, B. 89
Willems, M. 293
Wolf, W. 153
Wong, D. F. 604
Wong, M. D. F. 337
Wu, A. C.-H. 101, 518
Wu, C. 644
Wu, Q. 371, 421

X

Xanthopoulos, T. 415
Xu, J. 762

Y

Yakovlev, A. 16
Yan, K. 752
Yang, A. 720
Yang, A. T. 34
Yang, W.-S. 83
Yaoi, Y. 415
Yasuda, M. 246
Yasuura, H. 246
Ye, Y. 107
Yen, S. H.-C. 627
Yen, T.-Y. 101
Yim, J.-S. 83
Yuan, L.-P. 377

Z

Zhao, J. 141

Session Index

Panel: An Executive View of the EDA Industry

Session 1 - Sequential Synthesis

Session 2 - Interconnect Modeling

Session 3 - Novel Techniques for Software Scheduling

Session 4 - Embedded Tutorial: Tools and Methodologies for Low Power Design
Panel: Low-Power Design Tools: Where Is the Impact?

Session 5 - Simulation Techniques for Microprocessors

Session 6 - Combinational Logic Synthesis

Session 7 - Interconnect Parasitic Extraction

Session 8 - Advances in Timing Analysis for Embedded Software

Session 9 - Applications of Formal Verification

Session 10 - System-Level Exploration and Refinement

Session 11 - Binary Decision Diagrams

Session 12 - Timing Analysis

Session 13 - Embedded Tutorial: Code Generation for Core Processors

Session 14 - Panel: Physical Design and Synthesis: Merge or Die!

Session 15 - System-Level Optimization and Verification

Session 16 - Formal Verification

Session 17 - Analog Simulation

Session 18 - Software Synthesis for Embedded Systems

Session 19 - Experiences in System Design and Education at Universities

Session 20 - Standard Cell and Physical Design Methods

Session 21 - Modeling and Transformations in Synthesis

Session 22 - Statistical Power Estimation Techniques

Session 23 - Co-Simulation

Session 24 - Panel: Challenges in Worldwide IP Reuse

Session 25 - Emerging Technologies and Architectures for Low Power

Session 26 - High Level Synthesis for Low Power

Session 27 - Module Generation

Session 28 - BIST and DFT

Session 29 - Panel: Hardware/Software Co-Verification

Session 30 - DSP & Telecommunication System Design

Session 31 - Embedded Tutorial: High Level Power Modeling, Estimation, and Optimization

Session 32 - Advances in Partitioning

Session 33 - Processor Test Techniques

Session 34 - Panel: The Next Generation HDL

Session 35 - Design Processes and Frameworks

Session 36 - Probabilistic Models of Input Data for Efficient Power Estimation

Session 37 - Hot Topics in Routing

Session 38 - Test Generation and Fault Simulation

Session 39 - Panel: The Road Ahead in CPLD & FPGA Design Methodology

Session 40 - Deep Submicron Modeling and Analysis

Session 41 - Technology-Dependent Optimization for Performance and Power

Session 42 - CAD Issues for Micro-Electro-Mechanical Systems

Session 43 - Hardware/Software Partitioning

Session 44 - Embedded Tutorial: Chip Parasitic Extraction and Signal Integrity Verification
Panel: Noise and Signal Integrity in Deep Submicron Design

Session 45 - Designing High Performance and Low Power Microprocessors Using Full Custom Techniques

Session 46 - Formal Verification Techniques

Session 47 - Placement Techniques

Session 48 - Panel: The EDA Startup Experience: Financing the Venture

Session 49 - Heterogeneous System Analysis