A Low Power Switching Power Supply for Self-Clocked Systems[1]

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Abstract *- This paper presents a digital power supply controller for variable frequency and voltage circuits. By using a ring oscillator as a method of predicting circuit performance, the regulated voltage is set to the minimum required to operate at a reference frequency which maximizes energy efficiency. Our initial test silicon, implemented with a fixed frequency controller, is analyzed and reveals that the controller's power consumption is a major limitation for such a design. To make the controller power dissipation scale with the CV^2f power of the load, we introduce a new architecture with variable frequency control, which allows the controller's supply and frequency to scale along with the load device.*

Introduction

Power consumption in clocked digital CMOS circuits is dominated by dynamic power dissipation, and is given by:

$$P_{dynamic} = \alpha \cdot C_{Tot} \cdot Vdd^2 \cdot f_{clk}$$

where α is the activity factor, C_{Tot} is the total switched capacitance, Vdd is the supply voltage and f_{clk} is the clock frequency. While α and C_{Tot} are generally fixed for a specific application, reducing supply voltage and clock frequency can result in dramatic power savings. A self-clocked system [1]-[3] achieves maximum savings by lowering the power supply voltage until the chip can just meet the specific performance requirements (desired clock frequency). Building such a system requires two components different from a conventional fixed voltage synchronous system: a method of dynamically predicting the chip's performance at different operating voltages and an adaptive power supply regulator.

A number of researchers have proposed using a delay chain/ring oscillator to match the critical path of a circuit, and using the frequency of the ring as an indicator of the chip's performance [2],[3]. The chip and the oscillator are built on the same die so that they closely track over process, temperature and voltage. This paper explores the design of the other component that is needed in these self-clocked systems: an adaptive supply regulator.

While many papers have been written on building efficient power converters [4],[5] to reduce power consumption, power supply regulators for self-clocked systems provide interesting new opportunities and constraints. The largest difference from conventional regulator design is that the inputs to this controller arrive as two oscillator frequencies in digital form. This makes a digital control loop appealing, since no A/D conversion is required. Furthermore, if the digital controller can use the same frequency and voltage as the circuit being supplied, its power will scale with the load current, making the converter efficient over a wide operating range. This range is needed since the chip power is likely to vary with the supply voltage to the third or higher power (since the operating frequency falls as the supply voltage decreases). This paper describes the issues and trade-offs with this type of adaptive supply regulator, and shows how an efficient converter can be built.

The following section starts by reviewing the issues in designing a switching power supply, and then describes the overall architecture, including the conflicting constraints that the designer must try to satisfy. The section discusses both the difficulties with using an adaptive supply and the limitations of the fixed frequency architecture which we initially built. Analysis of the measured data has led us to develop an improved architecture, which is described in a following section. In the last section, we reevaluate the use of a digital controller and conclude that this design approach holds promise for self-clocked systems.

Architecture

An adaptive power supply regulator consists of the following three main building blocks: a power converter, a mechanism for predicting circuit performance, and a controller. A standard 'buck' converter circuit [4], shown in Figure 1, is employed for efficient power conversion. The output of this type of converter is simply the average voltage of a pulse-width modulated (PWM) square wave, supplying power to the load. Since the averaging is done by ideally 'lossless' components (the L and C) acting as a low-pass filter, the power delivered to the load is close to the power that is pulled from the original supply (BVdd). Losses in this type of converter come from many sources: resistive losses in the

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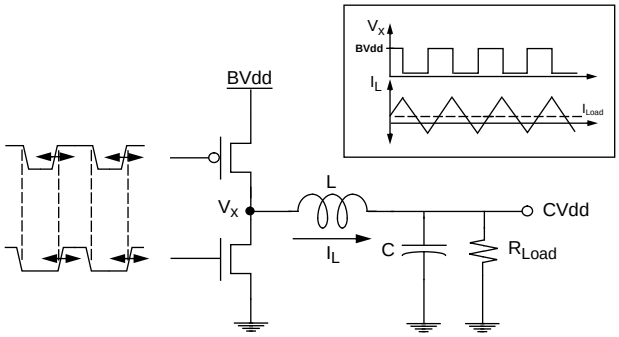
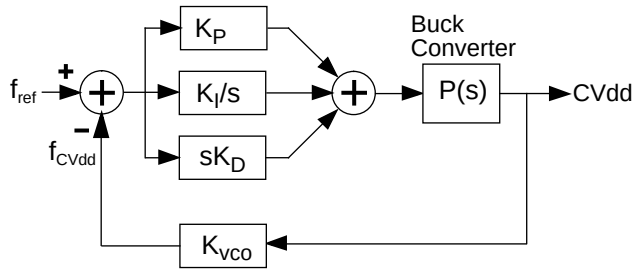
transistor switches, capacitive losses due to charging of the transistor gates and parasitic capacitances, short circuit current through the transistor switches, and parasitic losses of the filter's inductor and capacitor. Additional power is consumed by the buffers required to drive the CMOS power transistor switches. For very low power conversion, the power needed to operate the controller is also significant.

FIGURE 1. Buck Converter



In order to regulate the output voltage, the duty cycle of the square wave to the buck converter is set by a feedback control loop, which tracks CVdd with respect to a reference. A difficulty associated with designing this controller arises from the LC resonance of the buck converter. From an open loop frequency response analysis, a resonant peak at the cutoff frequency of the LC filter is observed. A sharp peak, quantified by the quality factor (Q), is desired for efficient power conversion. With a simple integral control, this resonant peak must be kept below unity gain in the open loop frequency response to ensure stability. As a result, loop bandwidth must be set very low. Thus, a more complex proportional, integral and derivative (PID) control, as shown in Figure 2, is required for stability and improved transient response to load changes. The compensation zeros introduced by the proportional and derivative control allow us to set the unity gain point beyond the resonant peak, improving the transient response, and eliminating the limitations due to the Q of the resonant circuit.

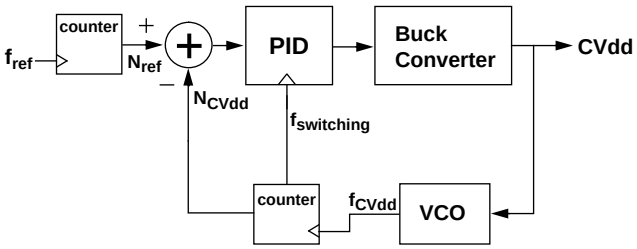
FIGURE 2. Control Loop Frequency Domain Model



Compared to an analog controller, a digital implementation imposes additional constraints on the design. Since the digital control is a sampled system, negative phase shift due to the delay through the loop adversely affects stability. This phase shift is linearly proportional to the bandwidth and inversely proportional to the sampling rate (which is equivalent to the switching frequency). While a higher switching frequency is desirable for smaller external filter components, voltage resolution requirements limit it. As a consequence, bandwidth must be traded for stability. For low power systems, however, a slower switching frequency is advantageous for reducing the converter's power consumption.

Another design constraint is power efficiency at low loads. A simple buck converter consumes a minimum energy each cycle. This is set by the CV^2 energy needed to switch the transistors, and the I^2R losses to support the current supplied, as shown in Figure 1. Current through the inductor is the sum of the load current and a ripple current (the magnitude of the ripple depends on the L and C parameters and the switching frequency). At low load currents, the I^2R losses from the ripple current through the inductor and transistors can limit efficiency. Thus, for high efficiency under low load conditions, the converter must both reduce its switching frequency (to reduce the CV^2 energy) and change from continuous to discontinuous mode of operation, eliminating losses due to circulating current in the LC circuit.

FIGURE 3. Original Architecture



Our initial approach for the control loop was a digital implementation that included variable frequency operation, support for low power operation, and used the adaptive regulated supply as the supply voltage for the controller itself. The original architecture is shown in Figure 3. The ring-oscillator frequency is used to 'run' the converter. It sets the switching frequency of the buck converter, and is also used as a time-base for the rest of the system. This ring oscillator, which also tracks the chip's performance, is counted over a switching period and compared with the reference frequency, also counted over the same period. A binary equivalent of the error between the two frequencies then feeds into the PID control block to make the appropriate corrections at the output. Thus, the output of the buck converter is regulated to the appropriate voltage for the load, modelled by the ring oscillator, to operate at the reference frequency. The digital implementation of the PID blocks uses shifters, adders and registers to mimic equivalent analog blocks. Since this digital control loop was

planned to operate at a variable frequency, if it is also run off the regulated supply, power consumption of the controller could be maintained at a constant fraction of the power delivered.

Taking advantage of the relative ease with which non-linear methods can be implemented in digital controllers, a pulse-squashing technique is used to further reduce power consumption of the converter. Given very low load conditions, ripple through the inductor can cause the total current to switch polarity, so that I^2R power is unnecessarily wasted through the power transistors. In order to minimize this power dissipation, when the controller detects current circulating back, subsequent pulses to the power transistors are squashed until the regulated voltage falls below some specified threshold. Current polarity through the power transistors is detected at the end of each switching period by momentarily turning off both NMOS and PMOS transistors and sensing the drain voltage. In addition to eliminating power dissipated by the circulating current, the buck converter's switching frequency effectively decreases, reducing the power consumed by switching the power transistors.

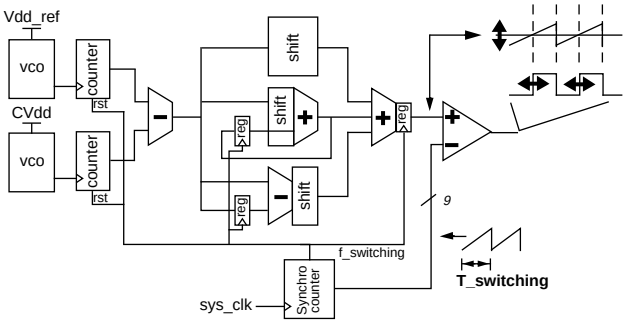
Although a variable operating frequency for the digital control loop is ideal for minimizing its power consumption, it is not ideal for loop stability. The PID time constants are proportional to the operating frequency while the complex poles of the LC filter are fixed, which makes the loop parameters vary with operating frequency. Given the additional constraint of the maximum ripple tolerable at the regulated supply, which is a function of the filter components' sizes and operating frequency, a stable loop over the dynamic range of the variable frequency could not be achieved. In order to verify the feasibility of a digital control loop and evaluate the performance of the rest of the system, we have opted for a fixed frequency control loop for our first test silicon. Instead of using the variable frequency output of the ring oscillator, a fixed external frequency is used to generate the operating frequency. The trade-off is that the fixed frequency digital control consumes a fixed overhead power and no longer tracks the power consumption of the load.

Our fabricated version of the switching power supply controller architecture consists of a PID control, operating at a fixed frequency, and utilizes a pulse-width-modulation technique with a buck converter to regulate the supply voltage with respect to a desired reference frequency. A non-linear pulse-squashing method is also implemented to reduce the controller's power consumption at low loads.

Test Chip

A block diagram of the test chip is shown in Figure 4. In order to facilitate transient response measurements of the loop, the test chip has been designed with two identical ring oscillators, where the reference frequency is set by a ring oscillator operating off a reference voltage. The output and reference voltages are converted to equivalent 9-bit binary values by counting the pulses out of the ring oscillators over a fixed switching period set by the output of the synchronous counter. The difference between the binary representation of the output and reference voltages feeds into the PID blocks. Shifters are used to set the appropriate gain coefficients for each of the control blocks. To avoid quantization error, the final adders are 16 bits, and incorporate additional bits created by the shifters. A subsequent output D/A conversion is implemented by comparing the binary representation of duty cycle, calculated by the PID block, to the output of the free running synchronous counter. The comparator generates a fixed frequency square wave whose pulse-width is modulated proportional to the varying output of the PID block.

FIGURE 4. Schematic of Digital Control



Measured Results

The digital PID controller was fabricated in a MOSIS 1.2µm CMOS process and tested with off-chip power transistors and filter components. Having verified loop stability, where CVdd tracks the input reference voltage, the performance of the supply was evaluated by measuring the power conversion efficiency and observing its transient response to a step in the input reference voltage.

FIGURE 5. Measured Conversion Efficiency

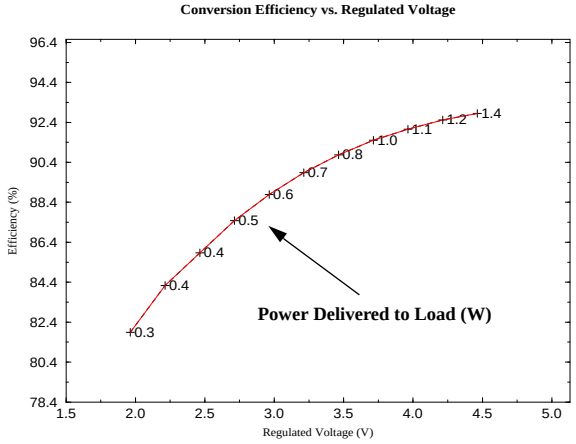
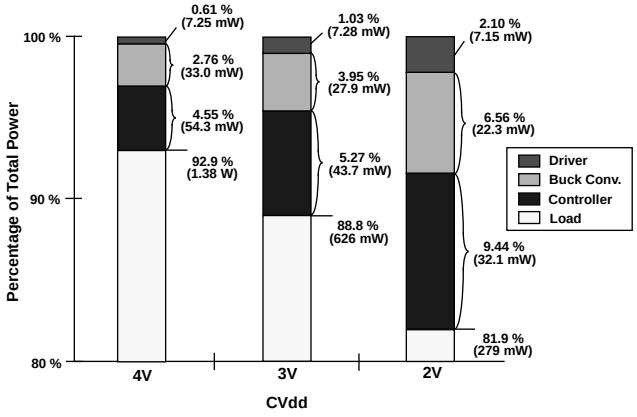


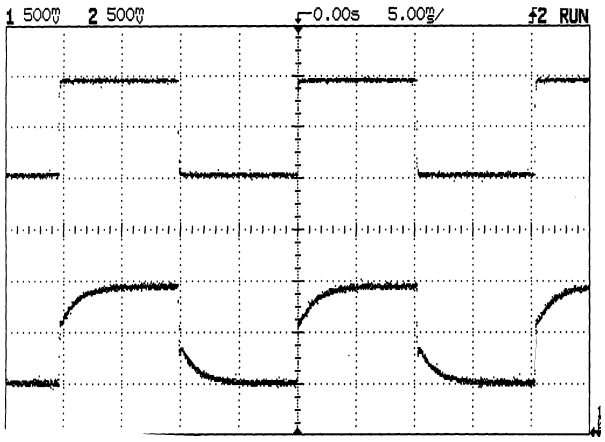
Figure 5 presents the measured results of the conversion efficiency with respect to different input reference voltages, and corresponding delivered power levels are also indicated. Although an actual application would have a capacitive load with a variable frequency clock, these measurements were performed with a resistive load to obtain a first order approximation of performance. With this configuration, the fabricated architecture achieves conversion efficiency greater than 90% while delivering 850 mW at 3.5 Volts. However, the efficiency rolls off at lower levels of regulated voltage and power delivered to the load, since the digital controller and buck converter consume some fixed overhead power. Figure 6 shows a decomposition of the different power consumption components as a percentage of the total power supplied to the power supply. As shown by the graph, the percentage of overhead power consumed increases as the regulated voltage (CVdd) decreases. The largest component of overhead power is due to the controller. While parts of the controller operating at the slow switching frequency could be powered off the regulated voltage, components operating at the high fixed frequency (sys_clk) and a fixed voltage (BVdd) consume a fixed amount of power. As was intended in the original design, this power can be reduced with variable frequency and voltage operation. An improved architecture, described in the following section, has been developed to achieve this goal. The next largest component of overhead power is due to the losses of the buck converter. This unavoidable component of overhead power can be further optimized with a more careful design of the converter, given specific power goals. Lastly, power consumed by the buffers driving the power transistors is indicated. Although the power saving achieved in the discontinuous mode is not reflected in the measured data presented, power can be reduced for low loads by squashing pulses which effectively reduces switching frequency.

FIGURE 6. Power Consumption Decomposition



The transient response of the stable control loop was obtained by using a square-wave as the reference voltage and observing the regulated output voltage waveform. The non-ideal response, shown in Figure 7, exhibits a rapid initial response to 60% of the final value and a slow settling time. This phenomenon, known as the doublet problem, is caused by the derivative control's zero close to, but not exactly cancelling out, the dominant pole. A discrepancy between the initial and final values of the pole-zero pair allows a fast initial response corresponding approximately to the loop bandwidth, but exhibits slow settling at the time constant of the dominant pole. This transient response limitation has been eliminated in the new design.

FIGURE 7. Regulated Voltage Transient Response



New Architecture

The key to improving efficiency while maintaining loop stability is to allow the internal frequency and voltage of the controller to change while keeping the controller's loop parameters relatively constant. Since these parameters are proportional to the update rate (or switching frequency) of the controller, it must be kept relatively constant (within a factor of two). To accomplish this, a frequency detection circuit is required. In the previous design, the switching frequency was set by the binary ramp wave, generated by a 9-bit synchronous counter, which was clocked with an external fixed frequency. In our new design, this counter is clocked by a variable frequency clock, and the number of bits that the counter counts up to is also variable. Thus, by detecting the frequency of the clock to the counter, the bits of the counter can be shifted to maintain a switching frequency which only varies by a factor of two. For example, when the frequency is half the maximum rate, the counter will only use 8 bits, restoring the switching frequency to the original rate. To further fix the loop parameters, the PID blocks' gain coefficients, implemented with shifters, can be dynamically adjusted within the factor of two change in frequency, limiting the loop parameters' excursions with frequency. By incorporating these two methods into the controller, a stable configuration for the loop can be achieved. This is verified by the simulated open loop fre-

quency response shown in Figure 8. A simulated transient response of the loop to step changes in the reference is also provided in Figure 9.

FIGURE 8. New Architecture - Frequency Response

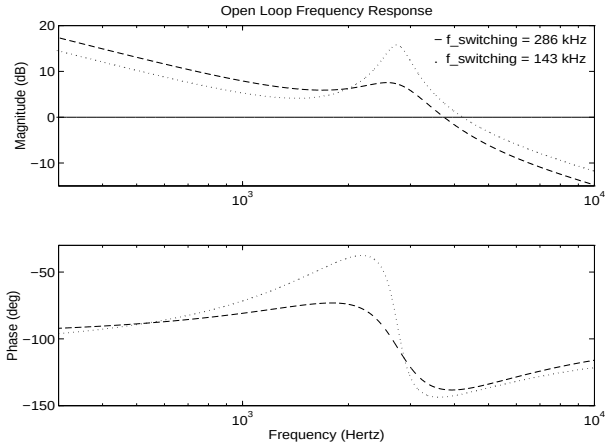
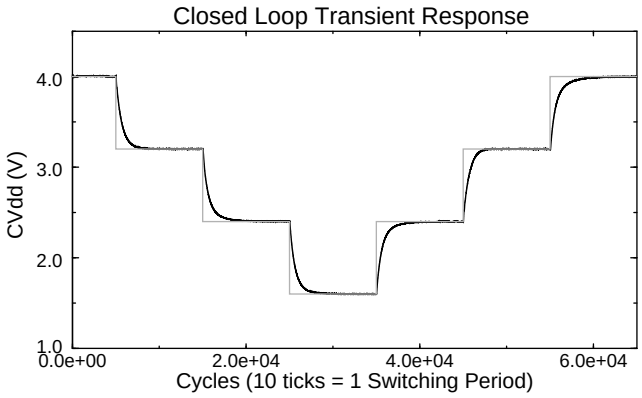


FIGURE 9. New Architecture - Transient Response



Given a variable frequency controller powered off the regulated supply, it is possible to keep the controller's power consumption overhead to a fixed percentage of the total power consumed. Components of the controller which operate at the switching frequency can also be powered off the regulated supply as long as the timing requirements of this much slower frequency can be met at the lowest regulated voltage level. Since this controller's power is nominally proportional to V^2f, we project that the power consumed should be on the order of 1 mW at 1.5 V and no longer be the dominant limitation of efficiency. For low voltage operation, the CV^2f power of the load should be sufficiently low so that the controller enters the discontinuous mode of operation and the buck converter's power and effective switching frequency are also reduced. Therefore, as long as the load is operating at low voltages, high conversion efficiency can be achieved. However, should the load enter into sleep mode and consume negligible amounts of power, a sleep mechanism for the controller is also needed to maintain efficiency.

Conclusion

In this paper we have explored the potential of designing a digital power supply controller for self-clocked systems to improve energy efficiency. A digital controller which can be embedded within the digital system to which power is supplied has the advantage of tracking the performance and power consumption of the rest of the system. The test silicon demonstrated the feasibility of a digital implementation, but showed that fixed frequency operation limited its effectiveness due to a fixed overhead power consumption. In order to maintain high conversion efficiency over a wide range of voltage and power, a variable frequency controller is required. By dynamically adjusting the switching frequency and gain coefficients to maintain relatively constant loop parameters, a variable frequency controller design which takes advantage of the power saving potential of self-clocked systems can be achieved. Since the switching frequency is not completely variable in this new design, however, overhead power consumed by the buck converter and buffers is a limitation for efficiency. Therefore, the discontinuous mode of operation, which effectively reduces switching frequency, is vital for maintaining efficiency at very low loads.

Acknowledgments

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