A Low Power High Performance Switched-Current Multiplier

D.M.W. Leenaerts, G.H.M. Joordens and J.A. Hegt
Dept. of Electrical Engineering, Eindhoven University of Technology
PO Box 513, NL 5600 MB Eindhoven, The Netherlands

Abstract- This paper presents an accurate switched-current multiplier, designed for 3.3V supply voltage, performing 0.625M multiplications per second with a maximum non-linearity of 0.94%. The used technology is 2.4μm n-well CMOS**.** The power dissipation is lower than 0.3mWatts.

I. INTRODUCTION

Current domain techniques and especially switched-current (SI) circuits are receiving more and more attention. Compared with switched-capacitor sampled-data circuits SI circuits have a number of important advantages: they are exclusively composed of MOS transistors, switches and current sources instead of opamps and precise linear floating capacitors, making them suitable for implementation in standard CMOS processes. Furthermore SI circuits are well suited for low-voltage and low-power applications.

Central element in this technique is the SI memory cell [1] allowing for short-term storage of currents. SI technique is often applied in filters, but its application area is rapidly growing [2] and comprises oscillators, DACs, algorithmic ADCs, Sigma-Delta converters, Cellular Neural Networks, etc. To the best knowledge of the authors this paper is the first proposal for a low power SI multiplier, being candidate for an essential elementary building block in many systems. Due to the SI technique, the multiplier has a low power dissipation.

ISLPED 1996 Monterey CA USA
0-7803-3571-8/96/$5.00 © 1996

A 3.3V supply voltage will be used.

Section II deals with the basic concept of (switched) current multipliers. In section III the actual implementation of the multiplier using the quarter-square principle is described. Experimental results are provided in section IV, while some concluding remarks are given in section V.

II. SWITCHED-CURRENT MULTIPLIER

There is a variety of existing current domain multiplier principles, such as the translinear multiplier and quarter square principle [4-9]. The latter principle to realize the multiplier is to utilize the following equation:

$$(x+y)^2-(x-y)^2=4xy. \qquad (1)$$

When both x and y represent currents, two current squarers are required which should be perfectly matched, in order to cancel the quadratic terms completely.

Application of a SI memory cell gives the possibility to reduce this to only one current squarer, as depicted in Fig. 1, circumventing the problem of matching. In this approach, first I_x and I_y are summed in the input circuit, the result is squared in the current squarer and temporarily stored in the memory circuit. In the next phase, I_x and I_y are subtracted, the result is squared and subtracted from the current that was stored in the memory circuit, resulting in an output current I_{out}, proportional to the product of I_x and I_y. This principle was used as a starting-point for the proposed SI multiplier. The SI multiplier of Fig. 1 is composed of three sub-circuits:

A. an input circuit,

B. a current squarer, and

C. a SI memory cell.

These three sub-circuits will be described in the next paragraphs.

A. Input circuit

It can be shown that, using Eq.(1), not all constant errors cancel by subtraction. For this reason a slightly adapted version of this principle was used, based on

$$(x+y)^2 - x^2 - y^2 = 2xy. \qquad (2)$$

This principle has two important advantages. First, the input currents of the current squarer during the clock phases are $I_x + I_y$, I_x and I_y . As no subtraction is needed anymore, these currents can easily be realized using only a few switches, without the need for a current inverter with its related error. Second, constant errors introduced by the current squarer can now completely be canceled. To do so, an extra clock phase is required in which no current is provided to the current squarer. It can be shown that in the end all errors are subtracted. In total four phases are required to perform the multiplication and therefore this multiplier is called a four-phase quarter-square SI multiplier. The input circuit can now be composed of only two transistors, switching the two input currents into the current squarer.

B. Current squarer

For the current squarer in Fig. 1 several circuits exist, such as presented in [8-10]. The latter circuit, see Fig. 2, was chosen for its simplicity. It has an (idealized) transfer of $I_m = I_o + \frac{I_i^2}{4I_o}$ in which I_o is a constant current, which depends on V_{bias} . The transfer function of the non-idealized current squarer of Fig. 2 can in first order be approximated as

$$I_m = I_o + e_1 + \frac{(I_i + e_2)^2}{4I_o}, \qquad (3)$$

with errors e_1 and e_2 being almost constant. These errors represent the output and input offset respectively. As explained in the previous section, these errors can be canceled with the slightly changed multiplier principle of Eq. (2).

C. Memory circuit

The third sub-circuit in Fig. 1 is a SI memory cell, for which several solutions exist [1-3]. The application of the accurate SI memory cell of Fig. 3 will be advantageous. Switching transistor S_2, which has the same size as S_1, and capacitor C_2 were added to reduce the clock feedthrough effects, caused by S_1. Cascode stage M_2, M_3 was added to reduce the effects due to the channel length modulation of M_1.

III. ACTUAL IMPLEMENTATION

The block diagram of the final multiplier is given in Fig. 4. In the first clock phase the term $I_x + I_y$ is squared and in the second and fourth phase the terms I_x and I_y respectively. In the third clock phase only a signal independent error is subtracted in order to cancel all introduced errors. However, this may not be essential for some applications, in which case three clock phases suffice. The final error will then be larger. The four phase sequence is equal to the sequence as defined in Eq. (2).

IV. EXPERIMENTAL RESULTS

In Fig. 5 the die photograph of the multiplier can be seen, occupying a 100x75 μm^2 chip area. The input currents as well as the output currents were measured by means of a 16-bits ADC. The measurements were performed at a conversion rate of 1.6μs, yielding 0.625 million multiplications per second. The internal clock frequency is 2.5 MHz. Fig 6 shows the absolute error compared to the expected transfer characteristic $I_{out} = aI_x I_y + b$ with a=4980 A^{-1} and b=4.022μA. The input current range is from -40 upto 40 μA, the maximum output current is 4.8μA. The power consumption is less than 0.3mW from a 3.3V supply. The total non linearity, defined as the absolute error divided by the maximum output swing, is specified as 0.94%. This value is similar to the simulated performance in [9] and measured performance of [10] but obtained at lower power supply voltages and low power. Because this is the first attempt of designing a multiplier in SI technique we can not compare this design to similar ones. Its -3-dB bandwidth is obviously much lower than time continuous multipliers and is approximately 100 kHz. Besides the low non linearity also the compactness of the circuit can be to advance in applications. Experiments show that increasing the conversion time by a factor 10 (i.e. approx. 50k multiplications/s), the non linearity reduces to 0.2%. This very low value is of interest in applications where speed is not the main design issue.

V. CONCLUSION

In this paper a SI multiplier was proposed, which basically consists of only one current squarer and two accurate SI memory cells. The problem of matching of two current squarers is circumvented and furthermore a number of non-idealities of the building blocks are canceled, resulting in an accurate multiplier in the current domain. Experimental results have been given to demonstrate the feasibility of the multiplier in SI design techniques. Advantages are the low power supply voltage, low power dissipation and the compactness of the design.

REFERENCES

[1] J.B. Hughes, I.C. Macbeth, and D.M. Pattullo, "Second generation switched-current signal processing," in *Proc. IEEE Int. Symp. Circuits and Systems*, pp. 2805-2808, May 1990.

[2] C. Toumazou, J.B. Hughes, and N.C. Battersby, "Switched-currents an analogue technique for digital technology," *IEEE Circuits and Systems Series*, Vol.5, London: Peter Peregrinus Ltd, 1993.

[3] D.Leenaerts, A.J. Leeuwenburgh, G.G. Persoon, 'High performance SI memory cell', Journal of Solid-State Circuits, Vol. 29, No.11, Nov. 1994, pp.1404-1407

[4] E. Seevinck, and R.J. Wiegerink, "Generalized Translinear Circuit Principle," *IEEE J. Solid-State Circuits*, Vol. 26, pp. 1098-1102, Aug. 1991.

[5] Liang-Yong Song, "A VLSI Design Methodology for Artificial Neural Networks," Univ. of Waterloo, Ontario, 1993.

[6] D.H. Sheingold, "Nonlinear Circuits Handbook," Analog Devices Inc., Norwood Ma., 1974.

[7] M.S. Piedade, and A. Pinto, "A new multiplier-divider circuit based on switched capacitor data converters," in *Proc. IEEE Int. Symp. Circuits and Systems*, pp. 2224-2227, May 1990.

[8] R.J. Wiegerink, "Analysis and Synthesis of MOS Translinear Circuits," Ph.D. dissertation, Univ. of Twente, Enschede, The Netherlands, 1992.

[9] S. Liu, C. Chang, 'CMOS Analog Divider and Four-Quadrant Multiplier Using Pool Circuits', *IEEE J. Solid-Sate Circuits*, Vol. 30, no.9 pp.1025-1029, 1995.

[10] K. Bult, and H. Wallinga, "Analog CMOS Computational Circuits," in *Proc. ESSCIRC'86*, pp. 119-121, Sept. 1986.

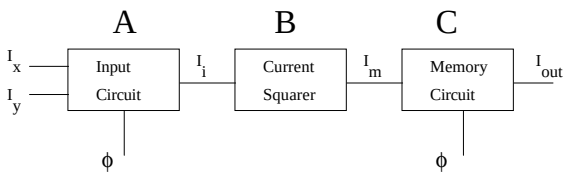

Fig. 1: block diagram SI multiplier.

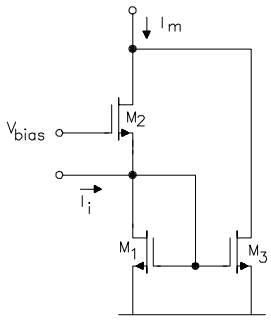

Fig. 2. current squarer

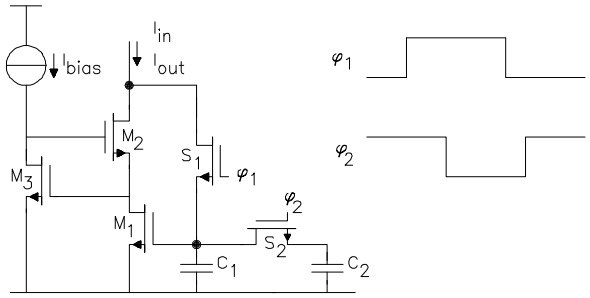

Fig. 3. accurate SI memory cell.

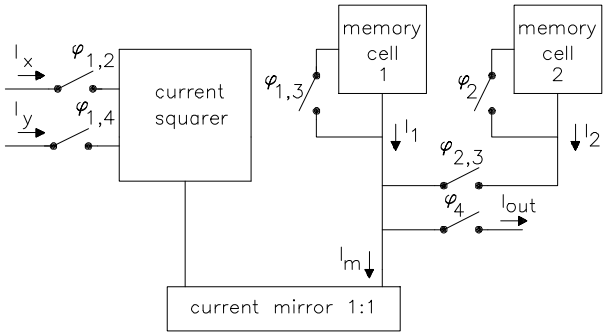

Fig. 4. block diagram four-phase quarter-square SI multiplier

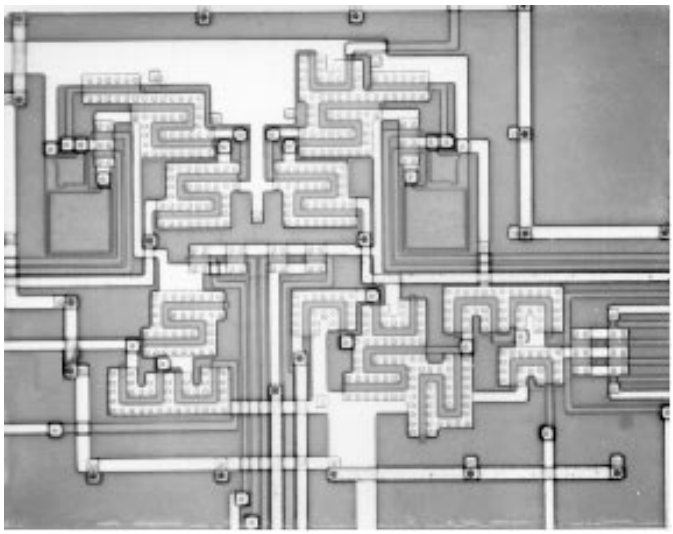

Fig. 5. Die photograph of the multiplier

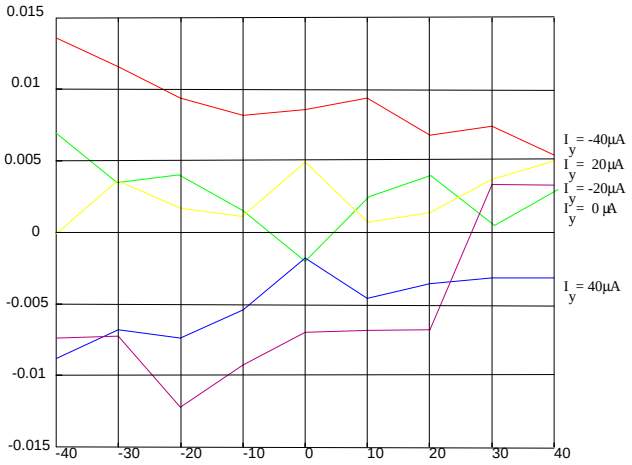

Fig. 6. Measured performances: absolute error (µA) versus input current for different currents I_y