

12-b 125 MSPS CMOS D/A Designed For Spectral Performance

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Abstract

A 12-b 125 MSPS, digital to analog converter fabricated on a 0.6 micron single poly double metal CMOS process is presented. The design operates on supply voltages from 2.7 to 5.5 volts and at 20 mA full scale output current consumes 150 mW from a 5 volt supply clocked at 100 MHz. Operating on a 3 volt supply, at 2 mA output current, and clocked at 60 MSPS, the power is less than 30 mW. New circuit architectures have been implemented which improve the spurious free dynamic range by 20dB over previous CMOS designs and matches the results of higher power bipolar and BiCMOS designs.

Introduction

Digital to analog converters built on low power CMOS processes have become very inexpensive and attractive for consumer communications applications. Previous CMOS D/A converters, mainly designed for video applications, have rather poor spectral purity. The transmit section of wired and wire-less digital communications systems place stringent demands on the D/A converter used. Time domain specifications like settling time and glitch impulse, which are important in video applications, are not always the best predictors of frequency domain performance.

Past experience with D/A converters has shown that delay differences between when a bit turns on and when it turns off results in a shift from the ideal 50% duty cycle and leads to even order (2nd, 4th ...) distortion components in the output spectrum. For a given time skew, the higher the output frequency the more pronounced the distortion. Time skews of as little as 10 picoseconds will result in a second harmonic as large as -60dB when the D/A converter is reconstructing output frequencies of greater than 10MHz.

This is clearly evident when recent CMOS and bipolar D/A specifications are compared[1][2]. The CMOS D/A has a spurious free dynamic range (SFDR) of 38.5 dBc for an output frequency of 20 MHz clocked at 80 MSPS, while the bipolar D/A has an SFDR of 51 dBc for an output frequency of 25 MHz clocked at 100 MSPS. The performance of both of these D/A converters are limited by the second harmonic. The CMOS design would seem to suffer from much larger timing errors than the bipolar design. The focus of this work was to understand the causes of these errors in the CMOS implementation and develop new approaches that reduce these errors.

A new current switch architecture has been developed which improves the SFDR of this CMOS design to 56 dBc for an output frequency of 25 MHz clocked at 125MSPS,

and when using the outputs in a differential configuration, the SFDR is 60 dBc. Again comparing these results to [1] and [2], there is a 17.5 dBc improvement over the previous CMOS D/A and a 5 dBc improvement over the bipolar D/A. In this improved design the second and third harmonic are now nearly the same and the SFDR is often limited more by the third harmonic at low frequencies.

Functional Description

The D/A, as shown in the block diagram figure 1, consists of a large PMOS current source array providing up to 20mA of total current. Segmentation is a well known technique used to reduce glitches in the output and improve linearity. The array is divided up into 31 equal currents which make up the 5 most significant of the 12 input bits. There are an additional 15 currents, each 1/16th of an MSB current, which make up the next 4 of the 12 input bits. The 3 least significant bits are binary weighted fractions of a middle bit current. Segmenting the five most significant bits was necessary to achieve 12 bit differential non-linearity (DNL) performance. The array is arranged to maximize the segment matching by spacing the 32 individual transistors that make up each segment equally around the array. A fixed shuffling of the order in which the segments are switched is also employed in the layout to breakup any remaining gradients that might exist. The devices for the segmented middle four bits are also distributed throughout the array to improve the match to the 31 MSB segments.

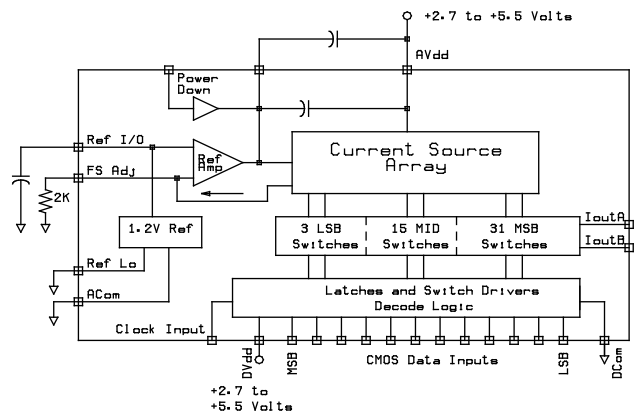


Figure 1 Block Diagram

The analog sections, which include a 1.2 volt band-gap voltage reference, operate over a 2.7 to 5.5 volt supply range. The full scale output current level is regulated by the on chip Ref Amp and is set by an external resistor. The full scale output current can be set from 2 mA to 20 mA. A power down mode turns off the output current lowering the power dissipation to less than 30mW from a 5volt supply.

The 49 currents that make up the D/A are switched to one or the other of the two output nodes, IoutA, IoutB, by 49 PMOS differential current switches. Logic for segment decoding and edge triggered latches make up the high speed digital interface. The digital logic section operates at the 125 MHz clock rate from 2.7 to 5.5 volts.

Latch and Switch Driver

Previous CMOS designs [3] have used latches and switch drivers much like that shown in figure 2. These designs have concentrated on the crossing point of the rising/falling waveforms on the gates of the output switches as a way to reduce the output switching glitch. This is certainly important in reducing the glitch caused if both switches are momentarily turned off. However, the delay or time skew between the two latch output signals due to the extra inversion in signal QB has not been considered.

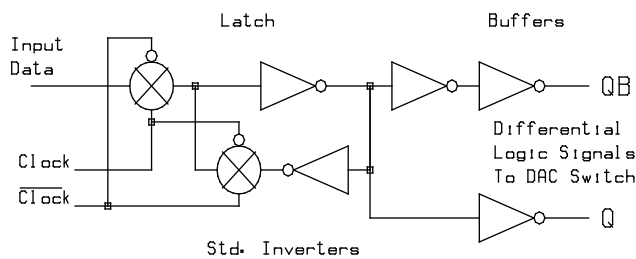


Figure 2 Previous CMOS latch

A previous design in BiCMOS [4] that addresses the problem of the mismatched delay is shown in figure 3. This arrangement has the property of creating the true and complement signals before the latch and using single transistor NMOS pass gates M1,2 to simultaneously pass these signals to a dynamic latch and on to the output switches through the buffers. Thus, there is no systematic delay between the Q and QB outputs of the latch. This insures symmetric switching and equally spaced output samples and greatly reduces even order distortion terms in the output spectrum. While this design does not suffer from the delay differences between the true and complement switch signals, it did not totally eliminate the output distortions present at the highest output frequencies. In this configuration, the binary-

weighted least significant bits of the D/A are created from a set of equal size currents which are scaled with an R/2R resistor network in the output. There are still significant timing delays arising from the non-negligible RC time constants of the network.

A CMOS implementation of the latch with the desired characteristics, shown in figure 4, has been developed [5]. The dynamic latch has been replaced with a cross-coupled weak-inverter static latch. As stated earlier, the least significant bit currents are binary-weighted making the R/2R resistor network in the output unnecessary. Therefore, this design does not suffer from the propagation delays which result from using a scaling network in the output and consequently has even lower harmonic distortion.

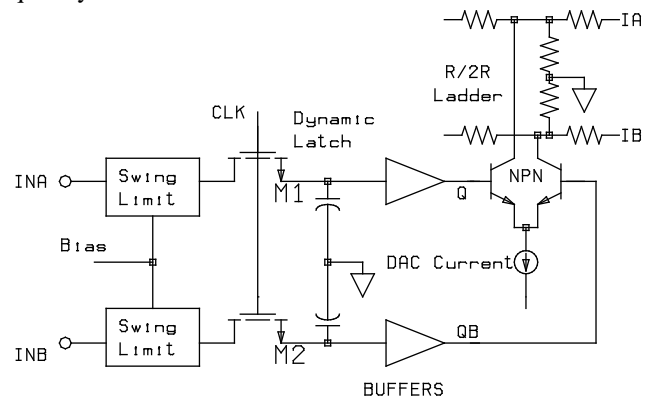


Figure 3 BiCMOS latch

Minimizing Power

Creating a design where the least significant bit currents are binary-weighted has the additional benefit of lowering the total current consumed in the current source array to just the total full scale current. In a design such as in figure 3, the total current used can be as much as twice the actual full scale output current. In this design, the supply current added by the band-gap reference, amplifiers and bias is about 4mA more than the full scale output current. When operated from 3 volts this is 12mW above the power necessary to drive the output load. The CMOS digital logic uses very little current at low clock frequencies.

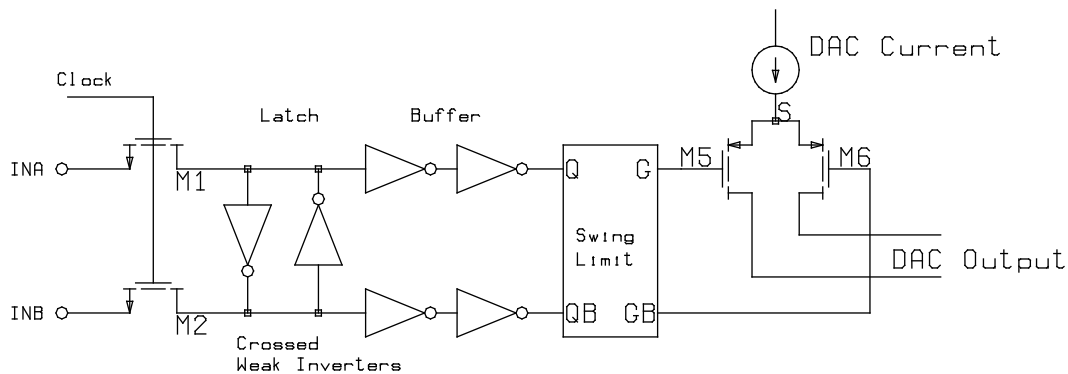


Figure 4 New CMOS latch

In this design, allowances were built in to operate over a wide range of power supply voltages and full scale output currents. The full scale output current is set with an external resistor. The reference amplifiers were designed to operate with wide input and output swings. This allows the output current to be adjusted over more than a 10 to 1 range.

Results

The design, built in 0.6 micron single poly double metal CMOS, resulted in a die size (including bond pads) of 1.65mm X 1.85mm. A photo of which is shown in figure 10. The DC linearity at the 12 bit level is +/- 0.6 LSB for differential non-linearity (DNL) and +/- 0.8 LSB for integral non-linearity (INL). Typical DNL and INL plots are shown in figures 6,7.

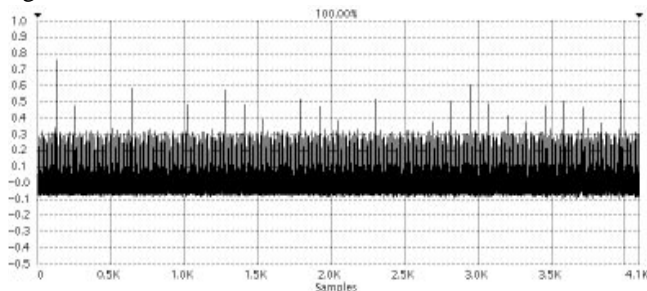


Figure 6 DNL

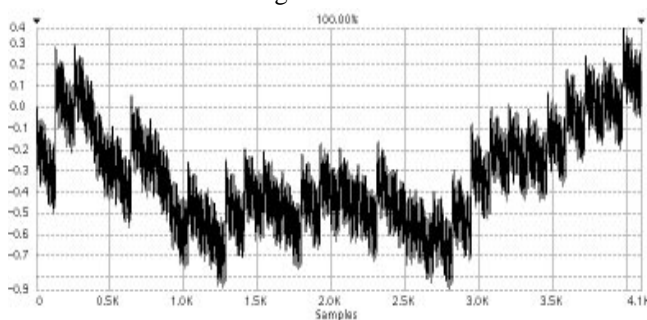


Figure 7 INL

While previous CMOS D/A converters provide both true and complement current outputs, due to the switching skews discussed earlier, the two outputs are not truly differential (in time) and using them in a differential configuration provides no improvement in the even-order harmonic distortion components in the output spectrum. This D/A has true and complement outputs that actually provide improved SFDR and harmonic distortion performance in a differential configuration. The best possible harmonic distortion performance is obtained when the outputs are combined with a transformer. Table 1 lists the SFDR results over the full $F_s/2$ bandwidth for various output frequencies at an F_s of 125 MSPS for both single ended and differential outputs. Figure 8 is a typical spectrum plot of a single full scale tone of 25 MHz at 125 MSPS.

Two tone and multi-tone performance is also critical for communications applications. Two tone tests results are also included in Table 1. The SFDR reported is with respect to

the amplitude of the tones (each at -6 dB), not the full scale of the D/A. Figure 9 is a spectrum plot of a multi-tone waveform with the D/A clocked at 50MSPS. The waveform consists of 20 tones starting at 3MHz that are equally spaced 0.9MHz apart up to 21MHz. The measured SFDR is greater than 60 dB.

Spurious Free Dynamic Range

at $F_s=125$ MSPS, $I_{fs}=20$ mA, 5volt supply, 150 mW

One Tone	Single-ended	Differential
1MHz	70 dBc	72 dBc
5MHz	63 dBc	70 dBc
10MHz	58 dBc	65 dBc
25 MHz	56 dBc	60 dBc
39 MHz	46 dBc	54 dBc
Two Tone		
12.5/13.5MHZ	60 dBc	62 dBc
25/25.125MHZ	54 dBc	60 dBc

TABLE 1.

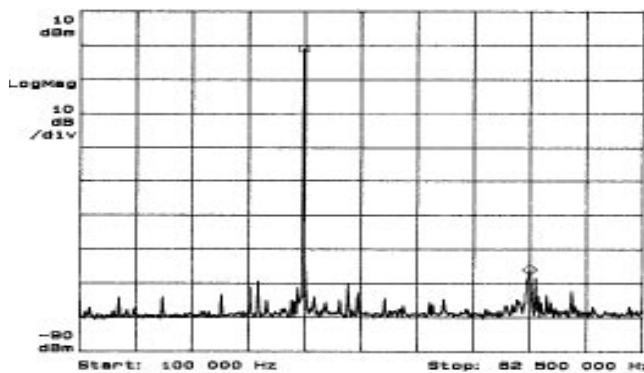


Figure 8 Single tone spectrum plot

The D/A can also be operated at much lower full scale output currents. With the full scale current set to 2mA and the power supply voltage lowered to 3 volts, the power consumed is less than 30 mW. Table 2 lists the results for various outputs in this lower power configuration. From the table, the maximum usable sample rate is reduced to around 60 MHz from the 125 MHz possible at full power.

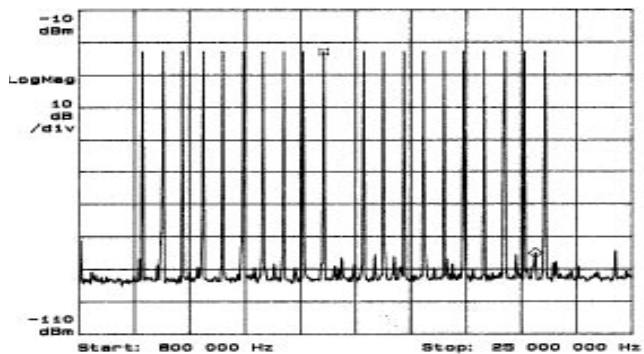


Figure 9 Multi-tone spectrum plot

Spurious Free Dynamic Range

$I_{fs}=2\text{mA}$, 3Volt supply, 30 mW

One Tone	Differential
1MHz, 10MSPS	76 dBc
2MHz, 20MSPS	73 dBc
4MHz, 40MSPS	62 dBc
6MHz, 60MSPS	58 dBc
8MHz, 80MSPS	48 dBc

Two Tone	Differential
2.0/2.15MHz, 40MSPS	70 dBc
4.0/4.3 MHz, 40MSPS	63 dBc

TABLE 2.

Conclusions

A complete 125 MSPS 12-b D/A converter with wide spurious free dynamic range has been demonstrated in 0.6 micron single poly double metal CMOS. Significant improvements in high frequency harmonic distortion have been achieved through the use of a new latch and switch driver design. The SFDR performance is equal to or better than bipolar designs which consume 5 times the power. 8-b, 10-b and 14-b versions of this D/A have also been implemented and are being investigated.

Acknowledgments

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References

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- [2]HI5721 10-bit 125 MSPS D/A converter data sheet, Harris Semiconductor, page 3-4, July 1995
- [3]S. Chin and C. Wu, "A 10-b 125-MHz CMOS Digital-to-Analog Converter (DAC) with Threshold-Voltage Compensated Current Sources", IEEE J. Solid-State Circuits pp. 1374-1380, Nov. 1994
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Figure 10 Die Photo

