FLOATING BODY EFFECTS IN PARTIALLY-DEPLETED SOI CMOS CIRCUITS

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Abstract— **This paper presents a detailed study on the impact of floating body in partially-depleted (PD) SOI MOSFET on various digital VLSI CMOS circuit families. The parasitic bipolar effect resulting from the floating body is shown to degrade the circuit noise margin and stability in general. In certain dynamic circuits and wide multiplexers, the parasitic bipolar effect is shown to cause logic state error if not properly accounted for.**

I. INTRODUCTION

Thin film SOI devices have recently received tremendous attention and drive in technology development because of its promise for low-power high-performance applications [1]. Partially-depleted (PD) devices, due to its ease of manufacturing, have been the front-up device choice [2]. The floating-body in the partially-depleted device has been known to introduce a kink in the DC I-V characteristics, lower the V_T at high drain bias, degrade the breakdown voltage, and cause hysteresis and instability during dynamic operations [3, 4, 5, 6]. Judiciously dropping body contacts in selected devices/circuits to eliminate the floating-body effect without severely degrading the density requires full understanding of the device behavior, circuit topologies, as well as their switching pattern dependency. This paper presents a detailed study on the impact of floating body in PD SOI MOSFET on various CMOS circuits. The complex interactions among the parasitic bipolar device, circuit topologies, and switching patterns are revealed and the resulting impact on circuit operation, stability, and functionality are explained.

II. DEVICE STRUCTURE AND CIRCUIT TOPOLOGY

The schematic cross-section of a partially-depleted SOI nMOSFET used in this study is shown in Fig. 1(a) [2]. The device has a 0.25 μm effective channel length, 5 nm gate oxide, 350 nm back oxide, and 140 nm thin silicon film. The device model used was developed by adding a parasitic lateral bipolar transistor, impact ionization, and back side capacitance to a bulk CMOS model. The parasitic bipolar model has been calibrated against detailed 2-dimensional device simulations. The equivalent circuit model is shown in Fig. 1(b). Note that the "core" nFET is the stripped-down FET model without parasitics.

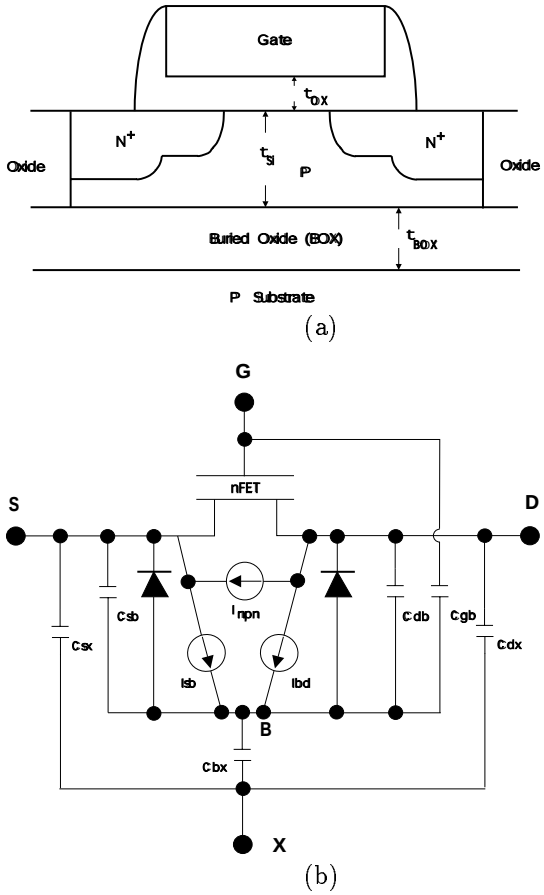

Fig. 1: (a) Schematic cross-section of a partially-depleted SOI nMOSFET, and (b) equivalent circuit model. (I_{npn} is the parasitic lateral NPN transistor collector current; I_{bs} and I_{db} are the internal EB abd CB junction diodes; I_{sb} and I_{bd} are the impact ionization currents.)

It is important to realize that the parasitic bipolar effect is very sensitive to the process and device details such as the silicon film thickness, source/drain junction depth, area, and extension, etc.. Hence, observations and conclusions based on any particular hardware and model should be taken qualitatively in their nature.

In floating-body configuration, the body potential is determined by the bias condition of the device, the capacitive coupling among the gate/source/drain/body volt-

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ages, the hole generation (in nMOS) by impact ionization, and generation/recombination in the space charge layer. Since the time constant for body charging by the impact ionization current is on the order of several ns [6], the body potential during the switching transient is primarily determined by the external biasing and capacitive coupling. For the parasitic bipolar effect to manifest during the circuit operation, the circuit topologies and switching patterns must be such that a large voltage is created/developed across the base-emitter junction of the parasitic bipolar transistor (i.e. a large voltage V_{BS}. across the body-source junction). For the SOI nMOS, this corresponds to the situation where both the body and the source are at "HIGH" to start with, and the source is subsequently pulled "LOW". For the SOI pMOS, the complementary situation would hold.

One circuit topology and switching patterns which encounter the aforementioned situation is the pass-gate (Fig. 2) [7, 8]. The basic configuration consists of complementary nMOS/pMOS switches gated by the control signal "C". Consider the case that after passing the "HIGH" state, "C" switches to "LOW" and the input (source) node is then pulled down. With the gate off and both the source and the drain nodes at "HIGH", the body will be at "HIGH" as well. Pulling down the input (source) node creates large forward bias across the base-emitter (body-source) junction of the nMOS device, resulting in large transient current through the parasitic npn transistor. For the pMOS, the complementary situation holds. But the parasitic bipolar effect is less pronounced due to the lower current gain of the lateral pnp transistor. The implications of this effect on various pass-gate based designs are studied in Section IV.

The other circuit topology susceptible to the parasitic bipolar effect is the stacked OR-AND CMOS circuit in Fig. 3(a). Consider the situation in which only the input to N1 is at "HIGH" (V_{DD} = 2.5 V) and the inputs to N2, N3, and N4 are all at "LOW" (Ground) at t = 0 (Fig. 3(b)). Node-1, the common source node of N1/N2/N3, sits at a voltage one V_T below the input to N1. The body voltages of N1/N2/N3 are all at "HIGH". When the input to N1 switches from "HIGH" to "LOW" at t = 0.6 ns, node-1 is capacitively coupled down slightly by the gate-to-source capacitance. The body voltage of N1 (V_{NB1}) is capacitively coupled down significantly by the large gate-to-body capacitance. The body voltages of N2 and N3, on the other hand, are only down slightly because their respective gate voltages remain unchanged and the voltage at node-1 is down only slightly. Hence, when the input to N4 subsequently switches (at t = 1.1 ns) to pull node-1 to ground, large V_{BS}'s are developed in N2 and N3 (not N1, since the body voltage of N1 has been capacitively-coupled down significantly), and significant parasitic bipolar currents flow through the supposedly-off devices N2 and N3 to pull-down the output node.

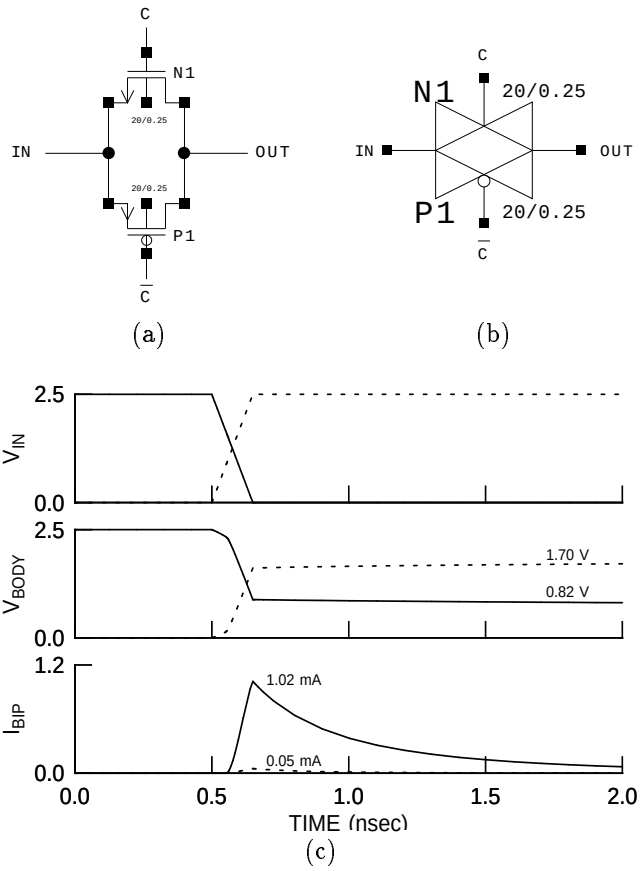

Fig. 2: (a) Basic pass-gate configuration, (b) circuit symbol, and (c) pertinent switching waveforms (solid lines for N1 and dotted lines for P1).

III. DIGITAL CMOS CIRCUIT FAMILIES

For the static CMOS circuit in Fig. 3, the pMOS path restores and holds the output by construct. The net effect is only a very small dip in the output voltage waveform and the extra power consumption due to the parasitic bipolar current. For dynamic circuits [9], the consequence can be much more severe. Fig. 4(a) shows a 4-way dynamic OR circuit. Notice that the stack formed by the logic transistors and the evaluation transistor resembles the OR-AND stack for the static circuit in Fig. 3. Assuming that in the precharge phase, the input to N1 is at "HIGH" and the inputs to N2/N3/N4 are at "LOW". The dynamic node-2 is at V_{DD}, and the common-source node-1 is at V_{DD} - V_T. The input to N1 switches at t = 0.6 ns from "HIGH" to "LOW" and the circuit subsequently evaluates at t = 1.1 ns. These switching patterns set up N2/N3/N4 in a condition similar to that discussed in the previous section, and large parasitic bipolar currents flow through these off devices to pull down the dynamic node-2 when the circuit evaluates. Depending on the strength of the feedback half-latch P1, the parasitic bipolar currents may produce a disturbance at node-2 and the output node, or completely upset and invert the logic state (Fig. 4(b)). Hence, the feedback half-latch has to be sized up (at the expense of circuit speed) to overcome this effect in the worst case situation.

The above potential hazard happens to all dynamic cir-

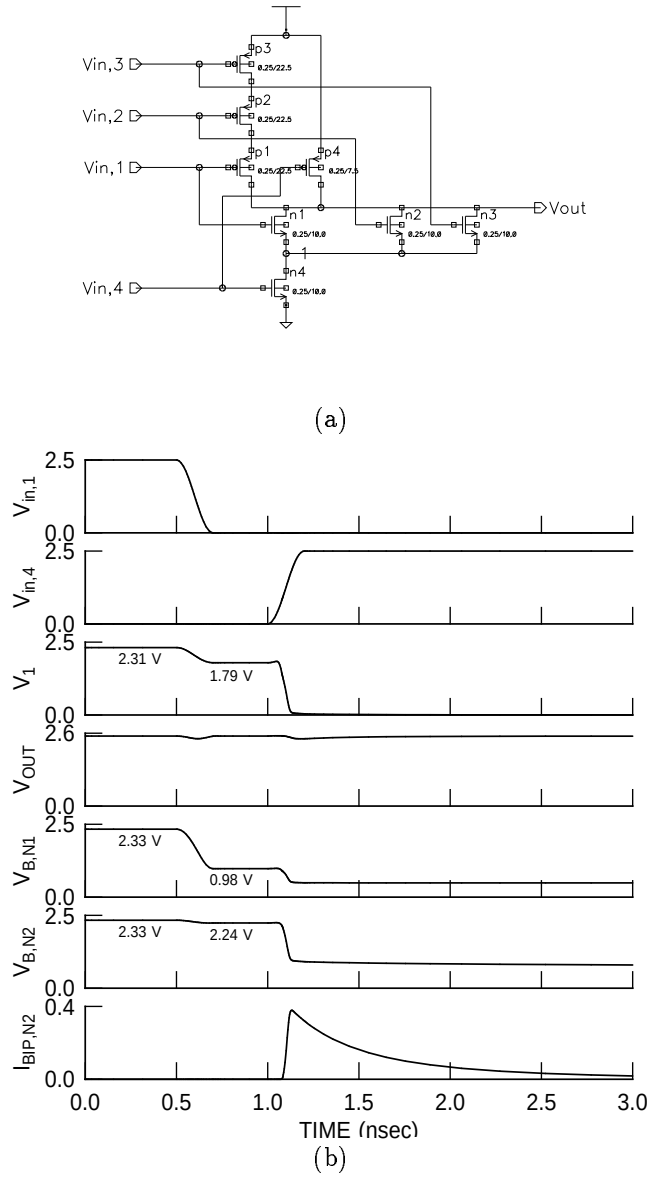

Fig. 3: (a) Static 3-way OR-AND circuit, and (b) pertinent switching waveforms.

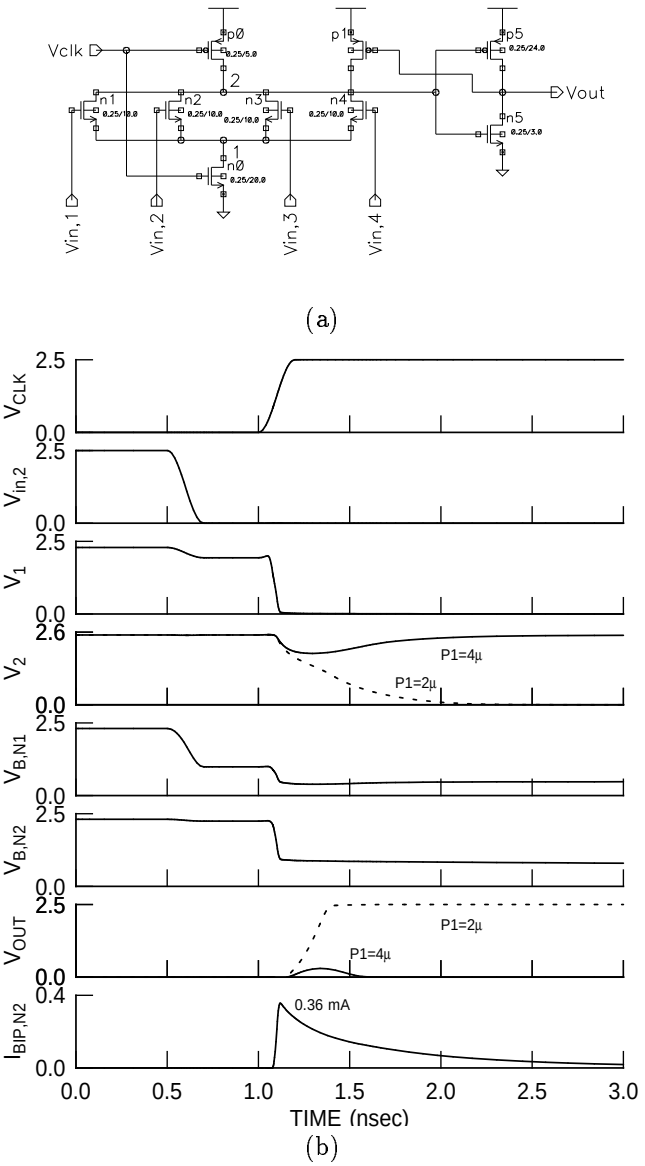

Fig. 4: (a) Dynamic 4-way OR circuit, and (b) pertinent switching waveforms.

cuits. Another example is the dynamic cascade voltage switch logic (CVSL) [9, 10] depicted in Fig. 5. The branch containing N1/N2/N3/N4 is the same as the nMOS portion of the static circuit shown in Fig. 3(a). The branch containing N5/N6/N7/N8 is the complementary branch. P0 and P1 precharge node-1 and node-2 to "HIGH" at standby. Under similar switching patterns and timing set up as in Fig. 4, parasitic bipolar currents flow through N2 and N3 to pull down the precharged node-1. If feedback half-latches (P11/P12) are not used or not properly sized up, wrong logic state would result at node-1, and the circuit settles in a (forbidden) state with both the true and complement outputs at "HIGH".

Some circuit blocks for data-flow design may encounter

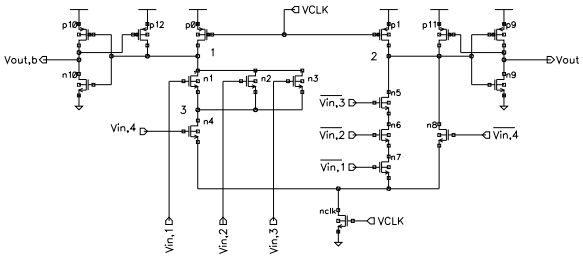

Fig. 5: Dynamic CVSL 3-way OR-AND circuit.

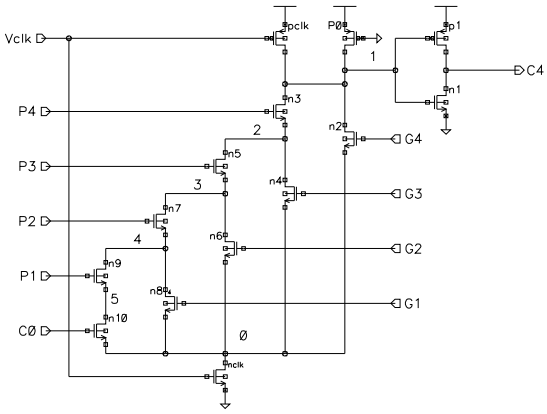

Fig. 6: Domino carry lookahead circuit

similar problem with parasitic bipolar effect. Consider a 4-bit domino carry lookahead circuit [9] for generating C_4 in Fig. 6,

$C_4 = G_4 + P_4\,(G_3 + P_3\,(G_2 + P_2\,(G_1 + P_1\,C_0)))$

where G_i and P_i are the generate signal and the propagate signal for the i-th stage respectively. Assuming that in the precharge phase, (G_4, G_3, G_2, G_1) = (0, 0, 0, 0), (P_4, P_3, P_2, P_1) = (1, 1, 1, 1), and C_0 = 1. Node-1 ($\overline{C_4}$) is precharged to V_{DD}. Node-0, the common-source node of N2/N4/N6/N8/N10 is at one V_T below the C_0 input. Hence transistors N2, N4, N6, and N8 are set up with their gate at "LOW", and drain/source/body at "HIGH". Assuming C_0 switches from "1" to "0" and then the circuit evaluates, the parasitic bipolar currents will flow through N2/N4/N6/N8 to pull down node-1, potentially causing the output node (C_4) to settle in the logically wrong "1" state.

Fig. 7(a) shows the Manchester carry chain circuit [9]. where the propagate signal (P_i) is used to gate the previous $\overline{carry}$ ($\overline{C_{i-1}}$) in a pass-gate configuration. Assuming that in the precharge phase, (G_4, G_3, G_2, G_1) = (0, 0, 0, 0), (P_4, P_3, P_2, P_1) = (0, 0, 0, 0), and C_0 = 1. Node-0 ($\overline{C_0}$), node-1 ($\overline{C_1}$), node-2 ($\overline{C_2}$), node-3 ($\overline{C_3}$) and node-4 ($\overline{C_4}$) are all precharged to "HIGH". Hence, all the pass-gate transistors N_{P1}, N_{P2}, N_{P3}, and N_{P4} are set up with their gate inputs at "LOW", and their drain and source nodes at "HIGH". When the circuit evaluates at t = 1.6 ns, node-0 is pulled down ($\overline{C_0}$ = 1), and parasitic bipolar current flows through the off pass-gate transistor N_{P1} to pull down node-1. As a result, parasitic bipolar current flows through the off pass-gate N_{P2} to pull down node-2. This chain parasitic bipolar effect, stemming from the series-connected pass-gate configuration, fades as it propagates down the pass-gate chain. Consequently, no significant parasitic bipolar current can be observed in N_{P3} and N_{P4}. Node-1 can be seen to be pulled down to 0.62 V and node-2 pulled down to 1.16 V, both low enough to cause errors in their logic states if they are buffered by

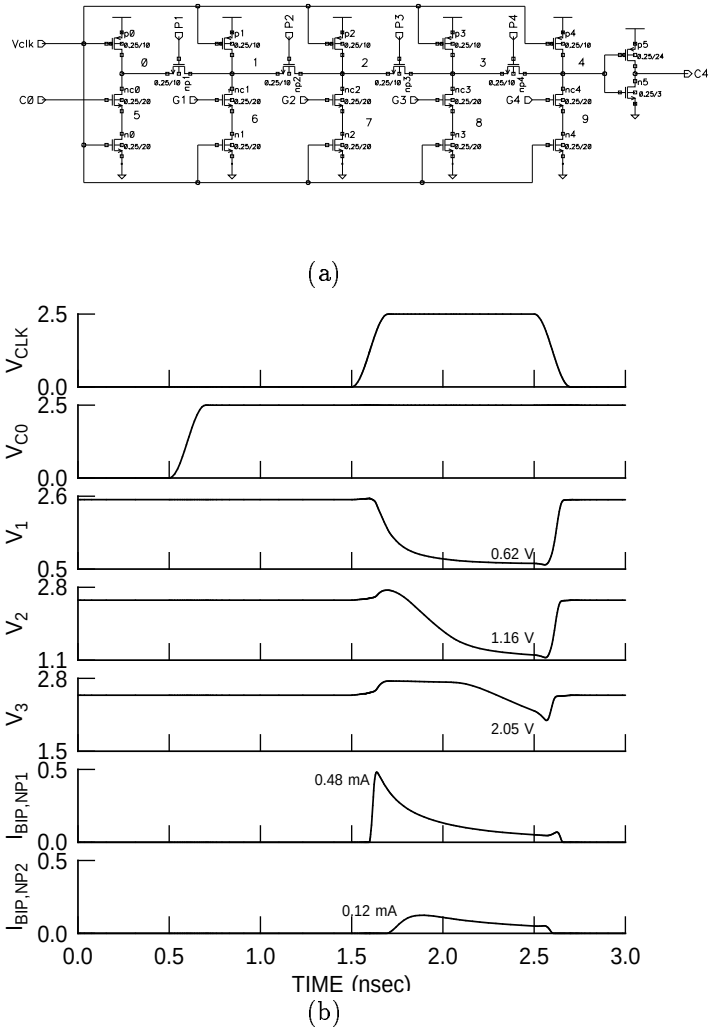

Fig. 7: (a) Manchester carry chain circuit, (b) switching waveforms for input patterns (G_4, G_3, G_2, G_1) = (0, 0, 0, 0), (P_4, P_3, P_2, P_1) = (0, 0, 0, 0), and C_0 = 1,

inverters for use in the subsequent logic. Node-3, because of the fading chain parasitic bipolar effect, is pulled down only to 2.05 V.

Depending on the input patterns, logic state error can also occur in the group-carry output C_4. For example, assuming that in the precharge phase, (G_4, G_3, G_2, G_1) = (0, 1, 0, 0), (P_4, P_3, P_2, P_1) = (0, X, X, X), and C_0 = X, where X can be either 1 or 0. When the circuit evaluates, node-3 is pulled down by the active transistor N_{C3} (G_3 = 1), resulting in parasitic bipolar current through the off pass-gate transistor N_{P4} (P_4 = 0). This parasitic bipolar current, being first-order (as opposed to the chain effect), is strong enough to pull node-4 down, causing the group-carry output C_4 to settle in the logically wrong "1" state.

IV. PASS-TRANSISTOR BASED CIRCUITS

Pass-transistor logic has been known for its efficiency in device use. The lower transistor count required to imple-

ment a given function improves the density, power and delay. This circuit style, however, is particularly vulnerable to the parasitic bipolar effect resulting from the floating-body as discussed in Section II. One of the most often and important application of the pass-gate is for the clock/timing control in various latch designs [9]. Fig. 8(a) depicts a L1/L2 type of latch with two non-overlapping clocks, C1 and C2. Consider the situation that after passing the "HIGH" state, C1 switches to "LOW" at t = 0 ns, and the input D is subsequently pulled-down at t = 1 ns as shown in Fig. 8(b). With C1 at "LOW", the pass-gate at the input to the L1 latch is supposed to be off, while the pass-gate in the feedback loop of the L1 latch is on to hold the state of the latch. Significant parasitic bipolar current, however, flows through the off nMOS of the input pass-gate for the case in Fig. 8(b), thus pulls down node-L1. Since the pMOS in the feedback inverter fights the parasitic bipolar current to restore node-L1. The result is a transient voltage dip (large enough to be a design concern) of node-L1 voltage (Fig. 8(b)). The complementary situation is less a concern because of the lower current gain of the parasitic pnp transistor.

Notice that in some high-density designs, the pass-gate in the feedback loop is removed and a 'trickle' inverter with small β devices is used [9]. It is important in this case to make sure that the trickle inverter has enough strength to overcome the parasitic bipolar current and restore node-L1, otherwise the latch may flip and latch into the wrong state.

Pass-transistor based wide multiplexers are another example of potential hazard due to the parasitic bipolar effect. The schematics of a pass-gate based n-to-1 multiplexer is shown in Fig. 9(a). In most applications, the control signals are 'orthogonal', selecting one and only one input at a time. Consider the worst case scenario for the parasitic bipolar effect as follows. Assume all inputs are at "HIGH" to start with, the selected input passes the "HIGH"-state to node-1 (and continues to hold the state of node-1 afterwards), and all the unselected inputs (n-1 of them) are then pulled down. As a result, parasitic bipolar currents flow through the n-1 nMOS in the n-1 unselected pass-gates to pull down node-1, which is being held/restored only by the single selected pass-gate. Fig. 9(b) shows the pertinent switching waveforms for n = 4, 8, 16, and 32. For n = 16, node-1 is pulled down to 1.36 V, close to the threshold of the output buffer (inverter), and a "bump" starts to surface in the output voltage waveform V_{OUT}. For n = 32, node-1 is pulled down to 0.78 V, decisively crossing the threshold of the output buffer, and the output voltage rises to 2.31 V. Since the parasitic bipolar current is a transient phenomenon, the selected pass-gate eventually restores the node-1 (and hence output) voltage. However, if the output is sampled and latched into the subsequent logic stages when it is "HIGH", wrong logic state would result.

The parasitic bipolar effect can also potentially lead to logic state errors in pseudo two-phase dynamic logic [9] as shown in Fig. 10(a). Consider the time period

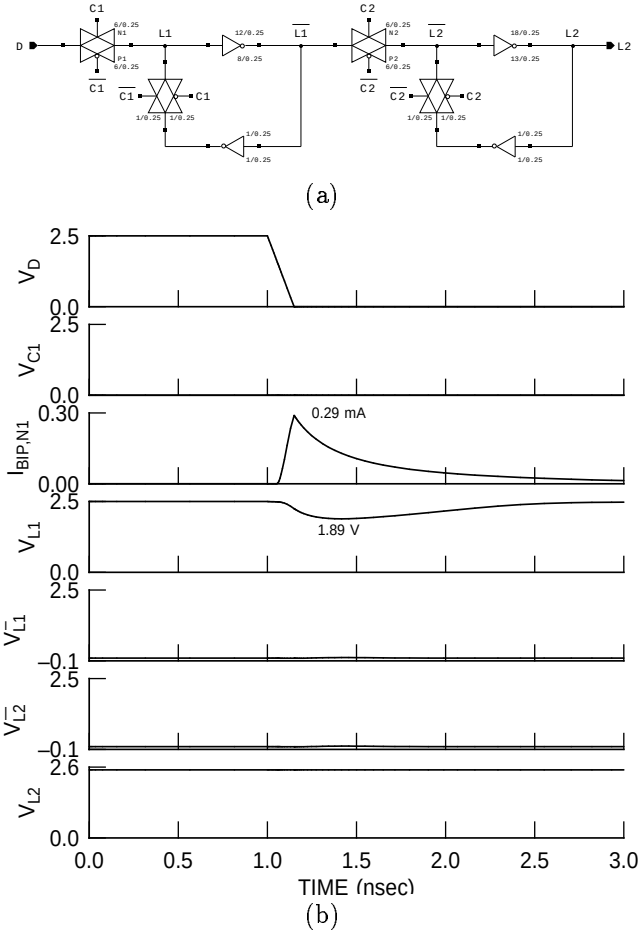

Fig. 8: (a) L1/L2 latch with two non-overlapping clocks, C1 and C2, (b) pertinent switching waveforms for parasitic bipolar current through the nMOS of the L1-latch input pass-gate.

when C2 is "LOW" (the other case when C1 is "LOW" is symmetrical). The pass-gate to the second stage is off and the second stage is evaluating. If the data stored in the gate capacitance (node-INT3) is "HIGH" and the first stage is evaluated to be "LOW" following the falling edge of C1, parasitic bipolar current flows through the nMOS in the off pass-gate, discharging the input (gate) node (node-INT3) from high to low. In Fig. 10(b), this nMOS parasitic bipolar current can be seen to completely discharge the gate node from 2.5 V to 0 V.

V. CONCLUSION

Parasitic bipolar effect in PD SOI MOSFET introduces noise sources to the circuit operation. For static CMOS circuits, the net is transient glitches in voltage waveforms and extra power consumption. For dynamic circuits, however, the parasitic bipolar effect is shown to degrade the noise margin and stability of the circuits. And depending on the circuit topology and switching pattern, it can lead to logic error if not properly accounted for.

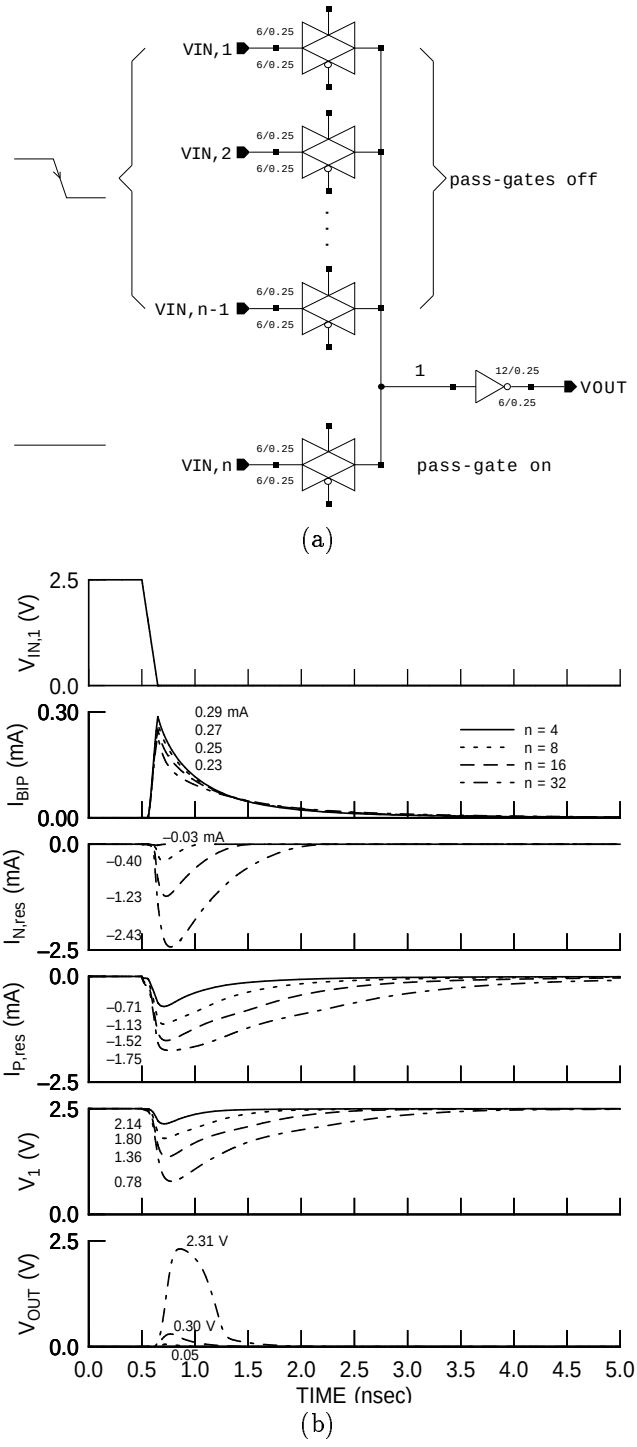

Fig. 9: A n-to-1 multiplexer: (a) circuit schematic, (b) pertinent switching waveforms for n = 4, 8, 16, 32.

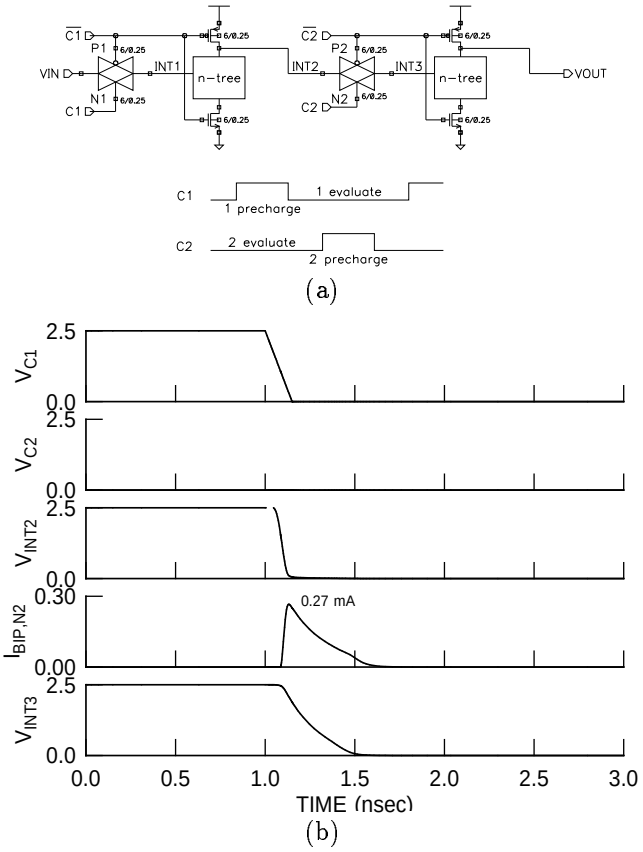

Fig. 10: A pseudo 2-phase dynamic logic circuit: (a) circuit schematic, (b) pertinent switching waveforms for parasitic bipolar current through nMOS N2.

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