Basic Experimentation on Accuracy of Power Estimation for CMOS VLSI Circuits

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Abstract

In this paper, we discuss on accuracy of several kinds of power dissipation model for CMOS VLSI circuits. Some researchers have proposed several efficient power estimation methods for CMOS circuits [1][2][3][4]. However, we do not know how accurate they are because we have not established a method to compare the estimated results of power consumption with that of actual VLSI chip. To evaluate the accuracy of several kind of power dissipation model such as chip-level, block-level and gate-level etc., we examined as follows : (i) Measuring power consumption of actual microprocessors. (ii) Estimating power consumption with several kinds of power dissipation model. (iii) Comparing (i) with (ii). The experimental results show as follows: (1) Power estimation at gate level is accurate enough. (2) Estimating power of a clock tree independently makes estimation more accurate.

1 Introduction

With recent popularizations in portable, battery-powered devices such as digital cellular telephones and personal digital assistants, minimizing power consumption of CMOS VLSI circuits becomes more and more important problem. Estimation of the power consumption is a key technology for low power VLSI circuits. Required methodologies for design of the low power VLSI circuits are following:

1. Estimating the power consumption as soon as possible in the design cycle.
2. Estimating the power consumption as fast as possible.
3. Promising the accuracy of power estimation.

To be satisfied with the above requirements, many researchers have proposed several efficient power estimation methods for CMOS circuits [1][2][3][4]. But it is still remaining as a question how accurate power estimations of large circuits are. There are few published reports on comparison of the estimated results of power consumption with the power consumption of actual VLSI chip. Few researchers used large circuit such as microprocessor for a power estimation. To make clear what is key technology of power estimation for very large circuits in the future, we consider on following questions with two actual microprocessors, KUE–CHIP2, a 8-bit non-pipeline processor, and QP–DLX, a 32-bit single-pipeline processor.

- How accurate an estimate of power consumption of CMOS VLSI Circuits.
- How do the power consumption models affect the accuracy of power estimation.

The paper is organized as follows: in section 2, target microprocessors architectures which are used in this study are presented. In section 3, we present three methods to measure power consumption of actual microprocessors, and measured results of power consumption. Section 4 explains several power dissipation models such as chip-level, block-level, pipeline-level and gate-level . In section 5, experimental results and consideration of the questions are discussed. Section 6 concludes the paper.

2 Target Processor Architecture

The target microprocessors used for our study are 8bit non-pipeline microprocessor KUE–CHIP2 and 32-bit single pipeline processor QP–DLX. In this section we present architectural features of these microprocessors.

2.1 KUE–CHIP2 Microprocessor

KUE–CHIP2(Kyoto University Education Chip2) is a 8-bit microprocessor designed for educational use in universities. KUE–CHIP2 was fabricated by European Silicon Structures(ES2) using 1.2 μm CMOS standard cell array technology, and internal memory with 512 bytes was implemented as a macro-cell. In this study, we do not use internal memory but external memory.

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Table 1: Specification of KUE–CHIP2

die size	$5.39 \times 4.59 = 24.70mm^2$
Combinational logic gates	1665(flip-flops 68)

2.2 QP–DLX Microprocessor

QP–DLX(Kyushu University Education Purpose DLX Microprocessor) is a 32-bit RISC microprocessor with five pipeline stages, and its basic architecture is presented in a well-known textbook by J.L.Hennessy and D. A. Patterson. QP–DLX was also designed primarily for educational use. QP–DLX was fabricated by European Silicon Structures(ES2) using $0.8\mu m$ CMOS standard cell array technology.

Table 2: HDL Description and its Logic- and Layout-Synthesis Results of Major Modules of QP–DLX

Block	SFL lines	Transistors	Area(mm^2)
IF stage	324	11,355	2.95
ID stage	728	18,666	5.23
EX stage	808	20,879	7.23
MEM stage	407	18,010	4.58
Register File	287	38,020	1.17
Total	3,521	121,572	66.24

3 Measurement of Power Supply Current

Power supply current varies irregularly and quickly in synchronous processors with CMOS technology. Quick and irregular variations in power supply current makes measuring power consumption of CMOS VLSI circuits more difficult.

It is difficult but necessary to measure power supply current without disturbing the original circuit behavior. There is some doubt about accuracy of power measurement. To confirm accuracy of power measurement of CMOS VLSI circuits, we compare three methods presented in succeeding subsection. In this section, we report results of measured power consumption of CMOS VLSI circuits.

3.1 Measuring Methods

The experimental equipments of the methods are illustrated in Figure 1.

Method1 A novel method to measure average power consumption of CMOS VLSI circuits with a large capacitor [8]. This equipment is based on a current regulator. The total amount of currents flowing out of large capacitor is measured without leakage. Power can be calculated by the current easily, because output voltage of this equipment is regulated (5[V]).

Method2 Measurement with the analog ammeter.

Method3 Measurement with a digital ammeter (Oscilloscope).

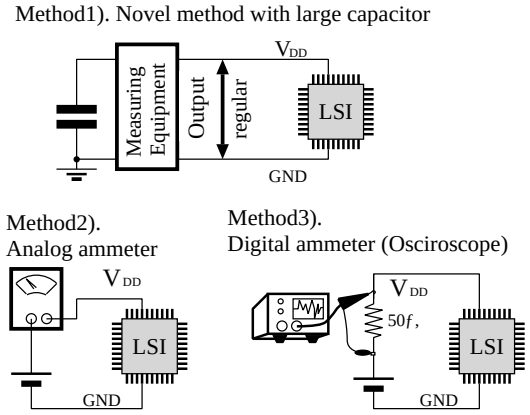

Figure 1: Measuring method

3.2 Accuracy of Power Measurements

Figure 2 shows results of power measurement of KUE–CHIP2.

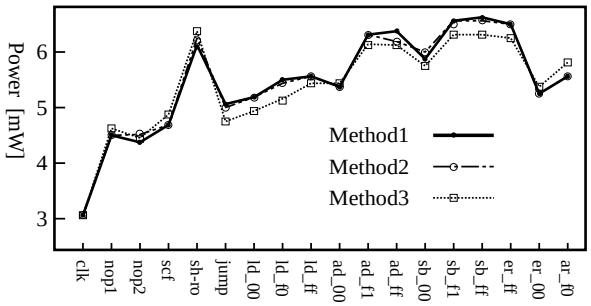

Figure 2: Comparison of Power Measurements of KUE–CHIP2

Figure 2 shows that measured values by three methods match very well. Hence, accuracy of measurement for CMOS VLSI is promised.

4 Power Dissipation Models

There are three major sources of power dissipation in CMOS circuits [10].

1. The leakage current $\cdots P_l$.
2. The direct-path short circuit current $\cdots P_s$.
3. The charging/discharging of load capacitances $\cdots P_c$.

P_c is generally the most dominant component. Estimating P_c, several models can be considered (Figure3). For a large and complex circuit it is often impractical to calculate the power dissipation in a detailed model. There may be a trade-off among accuracy, expense of compute and ease of extracting parameters for power estimation in these models.

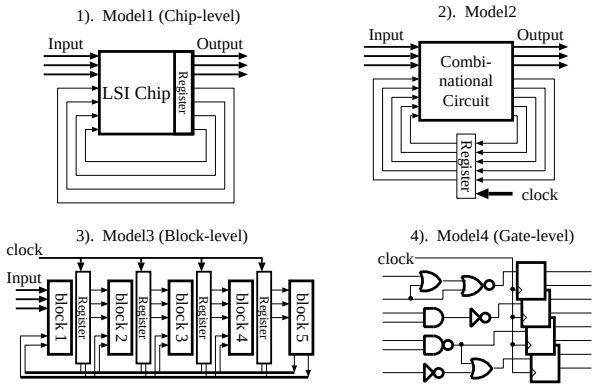

Figure 3: Power Dissipation Models to Estimate Power due to Charging/Discharging of Load Capacitance

Model1 This is a power dissipation model at the chip-level. Power consumption of a chip can be calculated in this model by estimating total load capacitance and average switching activities of the chip.

$$P_c = C_{chip} \cdot f_{chip} \cdot V_{DD}^2$$

Model2 In this model, we estimate power consumption of a clock tree, which is the most power consuming part, and other parts separately. This power dissipation model differs from Model1 only in this point. Power of the clock tree consists of power consumption of clock drivers and power due to charging/discharging routing capacitance of the clock tree and a clock input capacitance of flip-flops.

$$P_c = (C_{comb} \cdot f_{comb} + C_{clk} \cdot f_{clk}) \cdot V_{DD}^2$$

Model3 This is a power dissipation model at the block-level. Total power consumption calculated by estimating load capacitance and average switching activities of each functional block. Power consumption of the clock tree is estimated independently in this model too. We partition the processor chip into functional block as shown in Figure 4.

$$P_c = \left[\sum_{i=0}^{m} \{C_{blk}(i) \cdot f_{blk}(i)\} + C_{clk} \cdot f_{clk} \right] \cdot V_{DD}^2$$

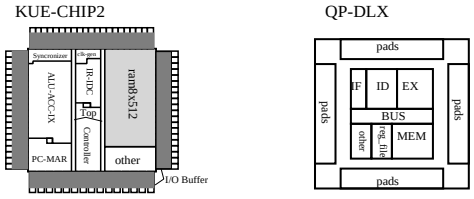

Figure 4: Floor Plan of KUE–CHIP2 and QP–DLX

Model4 This is a power dissipation model at the gate level. Switching activities of each node are obtained from switch level simulation. Load capacitance of each node is calculated from layout data.

$$P_c = \left[\sum_{i=0}^{n} \{C_{gate}(i) \cdot f_{gate}(i)\} + C_{clk} \cdot f_{clk} \right] \cdot V_{DD}^2$$

V_{DD} : The supply voltage.
n : The total number of gates.
m : The total number of blocks.
C_{chip} : The total load capacitance of a chip.
f_{chip} : The average switching activity of a chip.
C_{comb} : The total load capacitance of a combinational circuit.
f_{comb} : The average switching activity of a combinational circuit.
C_{clk} : The total load capacitance of a clock tree.
f_{clk} : The clock frequency.
$C_{blk}(i)$: The total load capacitance of the block(i).
$f_{blk}(i)$: The average switching activity of the block(i).
$C_{gate}(i)$: The load capacitance of the gate(i).
$f_{gate}(i)$: The switching activity of the gate(i).

5 Experimental Results and Consideration

We compare results by these four models with measured results of power consumption on KUE–CHIP2 and QP–DLX. Benchmark programs used in this experiments are infinite loops which are consist of single instructions. These instructions are shown at a horizontal axis in Figure 5 . In experiments, 1M[Hz] clock frequency was assumed.

5.1 Accuracy of Power Estimation

We report our results on KUE–CHIP2 and QP–DLX in Figure 5. Load capacitance of each partitioned block is calculated from layout data, and average switching activities of each partitioned block is calculated by switch level simulation. Consequently, only the size of partition can be a parameter of accuracy of power estimation in these models.

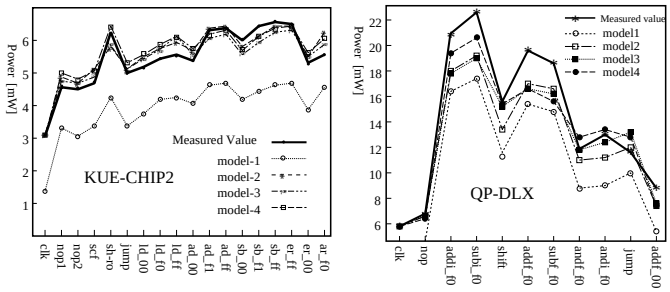

Figure 5: Comparison of estimation models on KUE–CHIP2 and QP–DLX

Figure 5 show that power estimation at gate level (Model4) is accurate enough. And estimating power of the clock tree and the other parts separately makes estimation more accurate. This is because switching activity and load capacitance of the clock tree are much larger than those of any other part of circuits.

It is hard to observe any relation between accuracy of estimation and size of partition on KUE–CHIP2. In case of QP–DLX, there is weak correlation between accuracy and the size of partition. This is because switching activity and load capacitance of each gates are not correlated in KUE–CHIP2, and weakly correlated in QP–DLX. Even though total load capacitance of the chip and average switching activity of the chip are estimated separately, power consumption can be calculated accurately. This result indicate a possibility of power estimation in earlier stage of design process. It is necessary for power estimation in earlier stage of design process to estimate average switching activity of the chip and total capacitance of the chip accurately from less information.

6 Summary and Future Work

In this paper, we evaluate the accuracy of power estimation for CMOS VLSI circuits by comparing the power consumption of actual chips with estimated values. Our experimental results show as follows.

1. Power estimation at gate level is accurate enough. Maximum error of estimation at gate level is only 12% on KUE–CHIP2, and 17% on QP–DLX. Accuracy of power estimation at gate level for CMOS VLSI circuits are promised.

2. Estimating power consumption of a clock tree independently makes estimation more accurate. This is because switching activity and load capacitance of the clock tree are much larger than those of any other part of circuits. We think that estimating power of bus line separately become more important for the power estimation in the future.

3. Even though a total load capacitance of a chip and an average switching activity of the chip are estimated separately, power consumption can be calculated accurately. This result indicate a possibility of power estimation in earlier stage of design process.

Future work will be devoted to make techniques estimating average switching activity of the chip and total capacitance of the chip from less information.

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