A 0.5V / 100MHz Over-V_{CC} Grounded Data Storage (OVGS) SRAM Cell Architecture with Boosted Bit-line and Offset Source Over-Driving Schemes

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Abstract

This paper proposes a 0.5V / 100MHz / sub-5mW-operated 1-Mbit SRAM cell architecture which uses an over-VCC grounded data storage (OVGS) scheme. The key target of OVGS is to minimize the charge amount supplied from the embedded charge pump circuits, which are required to boost the effective gate to source voltage (V_O=V_{GS}-V_T) up to 0.8V necessary to achieve 100MHz-operation even at 0.5V single power-supply. Thus, the key low-power strategy of OVGS is "putting the right (higher efficiency) boosted power-supply from charge pump circuit into the right position (less power consumed transistor) in a SRAM cell". This paper is focused on why OVGS can realize a greater savings of the charge amount supplied from the boosted power-line and can reduce the power dissipation to ≤ 1/30.4 and ≤ 1/3.9 compared to the previously reported negative source drive (NSD) scheme[1] and negative word-line drive (NWD) scheme[2], respectively, while achieving a 0.5V / 100MHz-operation.

I. Introduction

The negative source driving (NSD) scheme[1] has been recently reported as the centerpiece of sub-1V-operated high-speed SRAM cell architecture. This is because the source over-driving (V_L -> V_L') can be exploited to increase the effective gate to source voltage (V_O=V_{GS}-V_T) of the access and drive transistors, while maintaining the threshold voltage (V_T) of 0.6V, as shown in Fig.1. This enables a considerable reduction in the bit-line (BL) access delay ($t_{WL\text{-}BL}$) to ≤ 2.5ns, while preventing the subthreshold leakage current from booming, as shown in Fig.4.

However, even when exploiting NSD, there inevitably comes an increase in power-dissipation in the negative power-supply circuit (-Pump-C shown in Fig.2(b)), supplying -0.75V necessary to discharge the heavy loads of bit-lines and source-nodes at 0.5V-VCC. This is because of an intolerable degradation in the supply-efficiency (η_C) of -0.75V at 0.5V-VCC, resulting from the increase in the required number of pumping stage[3] necessary to achieve the target boosted-voltage, as shown in Table I.

On the other hand, to solve this, the negative word-line (WL) drive (NWD) scheme[2] has been recently proposed. NWD features as follows: 1) to use a strongly-low (i.e. negative) V_T (-0.3V) in the access transistor, in order to achieve V_O=0.8V, 2) pulling down the WL-reset level as far as to -0.9V in order to avoid the standby leakage from the BL to the source-node (V_L) even if using -0.3V V_T in the access transistor. However, unfortunately, NWD newly induces the problem of leakage from the boosted cell-power (V_H) line to BL, just when WL goes high (V_{WL}=0.5V), unlike when WL remains a negative level (-0.9V). This problem causes an intolerable large power dissipation in the +Pump-E, supplying 1.4V boosted cell power V_H (shown in Fig.2(c)).

Thus, to solve the above problems, while targeting for a 0.5V /100MHz /sub-5mW -operated 1-Mbit SRAM cell, we have newly developed an over-VCC grounded data storage (OVGS) scheme, based on the our recently proposed offset-source driving (OSD) scheme[4], which was optimized only for a 0.8V single battery-operated SRAM.

The key target of OVGS is to minimize the charge amount supplied from the embedded charge pump circuits, which are required to boost the effective gate to source voltage (V_O=V_{GS}-V_T) up to 0.8V, necessary to achieve 100MHz-operation even at 0.5V single power-supply. Why OVGS can realize a greater savings of the charge amount supplied from the boosted power-line is the focus of this paper. We discussed why OVGS can reduce the power dissipation to ≤ 1/30.4 and ≤ 1/3.9

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compared to the previously reported negative source drive (NSD) scheme[1] and negative word-line drive (NWD) scheme[2], respectively, while achieving a 0.5V/100MHz-operation.

II. 0.5V/100MHz SRAM Cell Strategy using OVGS

As shown in Figs. 1 and 2(a), the key concept of OVGS features as follows : 1) "potential-shifting by over-VCC" of the data storage-node pairs of "high" and "low" V_H/V_L (0.5V/0V -> 1.3V/0.65V) for the unselected cell, 2) "identical level-boosting" of the BL-precharging and WL-driving, 3) over-Vcc offset-source driving (0.65V -> 0V) when accessing the cell, 4) charge-recycling source-line control, making it possible to avoid the power-loss when resetting the potential of source-line (0V -> 0.65V), and 5) column-decoded source-line drive in word-line direction, enabling to realize a pseud cross-point access.

OVGS can meet the following requirements simultaneously : 1) minimizing the charge amount Q_{Total} supplied from pumping circuit (-Pump-C or +Pump-B) required for charging and discharging the heavy loads of BL-capacitance C_{BL} and source-node capacitance C_{SN}, as shown in Fig.5, and 2) avoiding the leakage I_{LK} from the boosted cell power node V_H to BL, which causes a large amount of idle charge dissipation in the pumping circuit (+Pump-E or +Pump-A), as shown in Fig.6.

(A) Minimizing charge amount Q_{Total} for source over-driving

The key to minimizing the charge amount Q_{Total} necessary for the source over-driving, supplied from 0.5V single power, is to use the GND line, instead of the negative power-line (V_L'= -0.75V), unlike NSD [1]. This is because the supply efficiency of GND (0V) is 100%, while that of negative power (-0.75V) is 10% at the most, as shown in Table I.

Furthermore, the charge amount for the negative source driving (Q_{SD}), is truly huge, compared with that of BL-precharging (Q_{PR}), as shown in Fig.5(b). (Note that Q_{SD} consists of 1) the charge (Q_{SL}) at 0.75V-swing on the total source-node capacitance (C_{SN}) of 256-cells connected in common and 2) the charge at ΔV=0.15V-swing on the capacitance (C_{BL}) of discharged BL.) In fact, Q_{SD} is 22-times larger than Q_{PR}. This is mainly based on the following reasons : 1) C_{SN} is 4.2-times larger than C_{BL}, and 2) the swing of source-line is 5-times larger than that of BL.

On the other hand, for the OVGS scheme, over-VCC potential-shifting of V_L up to 0.65V permits to use the GND-line for realizing a 0.65V source over-driving. This is reason why OVGS contributes to save the power dissipation in source over-driving. Furthermore, for the OVGS scheme, despite using the boosted power (V_{UPB}=0.8V) supplied from charge pump (+Pump-B) to precharge the BL-capacitance (C_{BL}), the charge amount Q_{Total} is reduced to ≤ 1/33 that of NSD. This is because of the following reasons : 1) Q_{PR} is less than 1/22 of Q_{SD}, and 2) supply efficiency (η_B) of 0.8V V_{UPB} is 15%, while that of -0.75V V_{DPC} (η_C) is 10%.

(B) Eliminating the leakage I_{LK} from the boosted cell power node V_H to BL

Our targeting SRAM must meet the following requirements for the access and drive transistors, composing the SRAM cell : 1) the effective gate to source voltage of V_O=0.8V, necessary to achieve the 100MHz-operation when selected, and 2) V_O= -0.6V necessary to suppress the subthreshold leakage current to 0.2µA even at 1M-bit cell array when unselected. To meet these, the OVGS scheme employs as follows: 1) the over-VCC source-offset (V_L=0.65V), 2) the low-V_T (0V) in the access transistor, 3) boosted cell power V_H (1.3V), and 4) identically boosted (0.8V) BL precharging and WL driving schemes, as shown in Fig.6(b). In these voltage-relations, 1) both of the boosted V_H of 1.3V and the source over-driving (V_L=0.65V -> V_L'=0V) contribute to achieve V_O=0.8V in drive transistor even using V_T=0.5V, when selected, and 2) over-VCC source-offset of 0.65V allows to use V_T=0V in access transistor, enabling to achieve V_O=0.8V combined with 0.3V-boosted WL (0.8V), while maintaining V_O=-0.75V when unselected, resulting from V_{GS}=-0.65V and V_T'=0.1V (after 0.1V-increased due to the body effect).

On the other hand, to meet these, the NWD scheme must introduce as follows: 1) a strongly low-V_T (i.e. negative, -0.3V) in the access transistor, 2) boosted cell power V_H (1.4V), and 3) negative-boosted WL driving (-0.9V) schemes, as shown in Fig.6(b).

However, unfortunately, NWD suppress the leakage only during standby period. On the contrary, when WL is activated, NWD newly induces the problem of leakage from the boosted cell-power (V_H) line to BL when WL goes high (V_{WL}=0.5V), unlike when WL remains a negative level (-0.9V), as shown in Fig.6(a). This problem causes a large power dissipation in the +Pump-E, supplying 1.4V boosted cell power V_H (shown in Fig.2(c)).

On the other hand, the OVGS scheme can solve the above problem by employing the identically boosted (0.8V) BL-precharging and WL-driving schemes, enabling to maintain V_O=0.8V in access transistor, even if using V_T=0V (i.e. no longer requires V_T=-0.3V), as shown in

Fig.6(b). The leakage I_O when WL goes high, can be reduced to $1/10^{3.5}$ compared to NWD at 100MHz-operation, resulting from the reduction in V_O (from 0.2V to -0.15V) , as shown in Fig.6. As a result, OVGS never requires a large power dissipation in the +Pump-A, supplying 1.3V boosted cell power V_H.

Regarding the rewriting of the V_H node from 0.7V (V_{CC}-V_T @V_{BS}=-0.7V) to V_{UPA} (1.3V) when write-access, the charge dissipation in +Pump-A can be neglected. This is because despite a supply-efficiency (η_A) of ≤ 10% as low as the case of +Pump-C (-0.75V), the charge amount for rewriting of the V_H node requires only 0.4% of that of NSD for source-node driving.

Furthermore, OVGS gives the advantage of access speed (9%-delay of t_{WL-BL} reduction as shown in Fig.7), resulting from the reduced junction capacitance C_j, dominating C_{BL}, due to the increased junction bias and increased drain-source current I_{DS} due to the increased V_{DS} by boosting the BL-precharging level.

(C) Charge-recycle over-V_{CC} offset source over- driving scheme

OVGS also features the column-decoded source-line (V_{SLm}, m=0-3) drive in WL-direction, enabling a pseud cross-point access. Each of V_{SLm} is connected to the common source-node of the drive transistor pairs every four cells in WL-direction, as shown in Fig.8. These V_{SLm} lines are laid out over the cell by using 3-rd metal without cell-area penalty. This contributes to suppress the increase in the charge dissipation, caused by supplying from charge-pump (+Pump-B) necessary to precharge the BLs, to 1/4 that of without this scheme. This is because OVGS reduces the number of cells connected in common to each V_{SLm} line and the number of BLs, discharged to GND, when WL goes high. OVGS suppresses the BL-swing of unselected cell (V_{SLm}=0.65V) to 1/256 of the selected cell (V_{SLm}=0V), resulting from over-Vcc offset-source potential of V_{VPL}=0.65V for unselected cells, as shown in Fig.8. This is reason why OVGS can realize the pseud cross-point access.

Another attractive point of OVGS is to realize the charge-recycling source-line control, enabling to eliminate the power-loss when resetting the source-line potential, as shown in Fig.9. The dumped charge Q_0 to virtual source-line V_{VPL} (t=t_0) is almost the equal to the required charge Q_1 necessary to reset the V_{SLm} line (0V -> 0.65V) (t=t_1) in the cycle at V_{CC}=0.5V, as shown in Fig.11. Thus, this implies that charge Q_0 is completely recycled to the charge Q_1 necessary to reset the V_{SLm} line.

Since the total capacitance (C_{VPL}) of V_{VPL} is 4096-times larger than C_{SSL} of V_{SLm} (e.g, V_{SL1-3} in Fig.8), the potential bounce ΔV_{VPL} is suppressed to only 0.2mV even just after Q_0 injection to V_{VPL} line. Thus, OVGS provides a stable source control necessary to realize the source over-drive and the pseud cross-point access without any power-loss.

III. Power Comparisons and Discussions

According to the simulated data of the 0.35μm 1M-bit CMOS SRAM, OVGS can save up to 1/30.4 the power of NSD at V_{CC}=0.5V, as shown in Fig.12(b). This is mainly due to the 97% reduction in the source and BL driving current consumption, which is the dominant factor of the SRAM-operating current, resulting from as follows : 1) eliminating the source-resetting current by using the charge-recycling source control, 2) avoiding to use the negative power(-0.6V) for BL-discharging, which inevitably induces over 90% supply loss, by shifting the potential range of the source-driving from (0V -> -0.75V) to (0.65V -> 0V), and 3) suppressing the swing of unselected BL to 1/256 by using the pseud cross-point access, as shown in Fig.10.

When compared against NWD, OVGS can save up to 1/3.9 the power of NWD at V_{CC}=0.5V, as shown in Fig.12(a). This is mainly caused by the elimination of the leakage current supplied from the boosted cell power V_H line, which causes 30mA supply current through the 0.5V single power-supply at 100MHz operation, resulting from maintaining V_T=0V in the access transistors by taking advantage of identically boosted (+0.3V) BL and WL schemes.

IV. Conclusion

Once targeting a 0.5V single battery-operated high-speed SRAM without an external power (e.g, -0.75V, 3V), the proposed OVGS becomes the most attractive candidate instead of NSD[1] and NWD[2] for suppressing the operating power to ≤ 5mW, while achieving a 64bit-100MHz operation at V_{CC}=0.5V and maintaining less than 0.2μA subthreshold leakage current for 1M-bit cell array (16K-word x 64-bit). This is because OVGS can minimize the charge amount supplied from charge-pump circuits, resulting from putting the boosted power-supply with higher efficiency into the less power consumed position of transistors in the SRAM cell.

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