Design for Manufacturability in Submicron Domain

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Abstract *- Key characteristics of newly emerging IC technologies render the traditional concept of die size minimization and traditional "design rules" insufficient to handle the design-manufacturing interface. This tutorial surveys the design and process characteristics relevant to the manufacturability of submicron ICs. The discussion also covers analysis of design for manufacturability (DFM) trade-offs. Yield and cost models needed to analyze these trade-offs are explained as well.*

1. Introduction

All IC design activities are driven by a vision of a designed circuit being manufactured and then applied to perform correctly the desired function. One can conclude, therefore, that "Design for Manufacturability" is a cliché, i.e., a meaningless term used to label design activities inherently belonging to the ordinary IC design procedure. And such conclusions have been supported by a large contingent of designers who neither have seen the need nor have had the luxury to perform manufacturability-oriented tuning of the designed circuits.

Designers haven't seen the need because of the powerful concept of design rules which have enabled the separation of design and manufacturing domains. Such a separation has facilitated an effective organization of design activities. It has also vastly simplified the algorithmization of the design process by successfully launching a CAD based IC design paradigm. On the other hand such a separation has allowed IC design to be practiced with less and less understanding of the involved physics. But physics ultimately decides the IC performance and economics of the fabricated circuits.

Designers have not had the luxury to explore manufacturability-oriented and process-based optimization for many reasons. One of them has been shorter and shorter time-to-market which does not allow time consuming process-design tuning [1]. Another reason has had a management background: the major responsibility of a typical design department has been timely deliver of first working silicon. Volume fabrication - the main source of revenue - has been the responsibility of the manufacturing department. Consequently, the design-process tuning has become a luxury for the designers and a burden for the technologist.

In such a situation design for manufacturability has been reduced to the minimization of die size and strict adherence to a given set of design rules. In some cases DFM has been reduced even further with the only level of freedom being a choice of elements from a library of pre-characterized cells. So, DFM has become a cliché with some level of relevance only for high volume IC's.

The objective of this tutorial is to argue that the above-described diminished role of DFM, suppressed by time-to-first-silicon mentality, is no longer acceptable in the era of submicron technologies. To achieve this goal this tutorial begins with a discussion of design objective functions derived from the main objective for both design and manufacturing - profit. Then a key DFM objective - manufacturing yield as a function of time - is discussed in detail. Next a short overview of the reasons for yield loss in submicron technologies is provided. The core of the tutorial is devoted to a discussion of DFM tasks and yield models which have to be addressed on all levels of design abstraction. A number of examples of DFM design problems illustrating important trade-offs are given as well. Finally, a simple DFM Roadmap for the submicron era is proposed.

2. DFM objectives

Reduced to its simplest form, the objective of IC design and manufacturing is maximization of profit. Fig. 1 summarizes the relationships determining the overall profit generated by a single product. Such profit is the difference between total cost and total revenue.

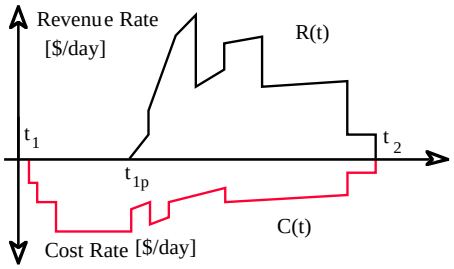

Figure 1. Revenue and cost rates as a function of time.

From a simple engineering perspective, the objective of design and manufacturing is to maximize the value of the integral:

$$\text{Profit} = \int_{t_1}^{t_2} [R(t) - C(t)]\, dt \qquad (1)$$

where:

R (t) and C(t) are rates of revenue and cost, respectively;

t_1 - t_2 is the "product life" from it's inception (t_1) to the end of fabrication (t_2).

To better understand the argument presented in this section, it is useful to examine both functions R(t) and C(t) a little bit closer. R(t), again in a simple but still relevant form, is a product of a sold volume of chips, V(t), and the unit price P(t). (See Figs. 2 c, d and e.) Note, however, that V(t) is a function of the number of processed chips (Fig.2a.) multiplied by the manufacturing yield Y(t) (Fig.2b). The latter is defined as the probability that the fabricated die passes final test. Hence:

$$V(t) = N_w(t)\, Y(t)\, N_{ch}(R_w, a, b) \qquad (2)$$

where:

N_w (t) - is the number of processed wafers

N_{ch} (R_W,a,b) - is a number of chips per wafer as a function of die dimensions a and b and wafer radius R_W [1,2].

The most important issue to see, however, is that R(t) is strongly related to Y(t), especially at the beginning of the manufacturing period (t_{p1}) when unit price is the highest. It is also useful to stress that R(t) is not only a function of time and the existence of competing products, but is also a function of a

"performance index". (Such an index for a microprocessor can be, for instance, clock frequency or a combination of clock frequency and power consumption.)

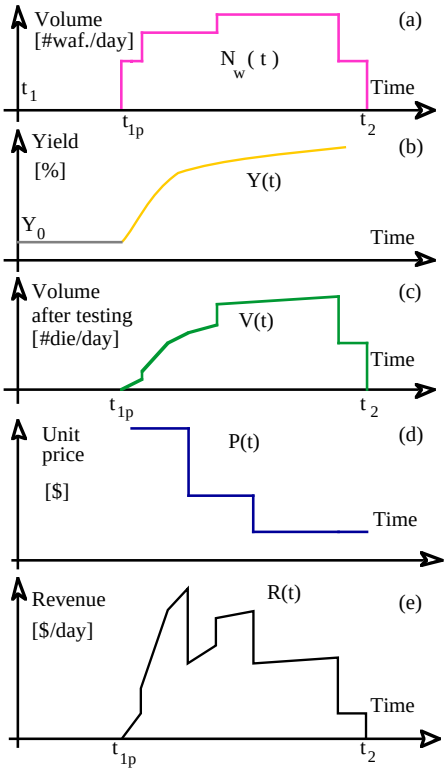

Figure 2. Revenue rate for a single product as a function of time.

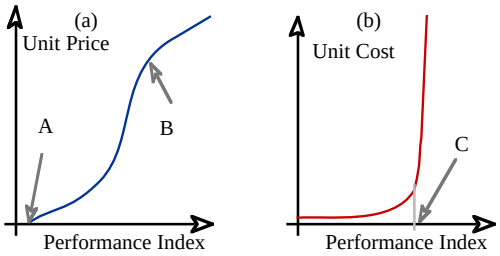

Figure 3. Average unit price and average unit cost as functions of performance index.

The performance index-price relationship is very complex and its approximation may exist in some form in the marketing/strategy departments of some leading IC houses. Here we illustrate the essence of the price-performance and then revenue-performance relationships by analyzing the average unit price (average of P(t) over $[t_{1p}, t_2]$ period of time) and the average unit cost (average of C(t) over $[t_1, t_2]$ period of time) as functions of the performance index. Fig. 3a shows a possible shape of the relationship between the average unit price and the performance index. It has two important attributes: the initial index level (point A), below which the product is worth nothing, and the beginning of a saturation range (point B), in which consumers begin to wonder whether they should pay a premium price for further performance increases. (Such points must exist because consumers eventually pay attention to the bottom line. For instance, when buying a portable PC, consumers typically care more about the battery weight-capacity ratio than a few more MHz of the microprocessor clock rate.)

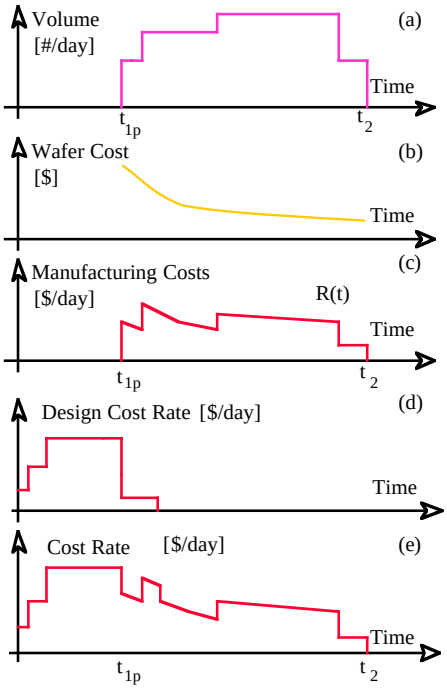

Figure 4. Cost rate for a single product as a function of time.

Fig. 3b. depicts the average unit cost as a function of the performance index. A key feature of this relationship is the abrupt increase in cost above a certain value of the performance index. It reflects the fact that for a given technology there is a performance limit (point C in Fig 3b) which cannot be exceeded regardless of allocated time and/or money. Of course, the average unit cost is a function of many other factors summarized in Fig. 4. Notice that C(t) includes cost of manufacturing and design (Figs. 4c and 4d) and that cost of manufacturing is a function of the number of processed wafers, $N_w(t)$, and cost of the wafer, $C_w(t)$ [1,3,4].

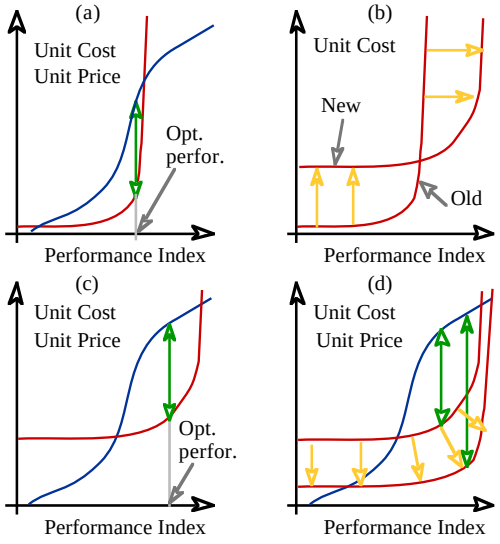

Figure 5. Performance based revenue optimization.

The two curves of Fig. 3 combined together can explain the essence of performance-based revenue optimization. The objective of such an optimization is to choose a performance index for which the price-cost difference is maximum. For the curves shown in Fig. 5a such a maximum is achieved close to the maximum performance index. And this has been very typical for a large portion of the IC industry.

The submicron era may, however, change this situation. The reason is the exponentially growing costs of manufacturing [1,5]. This growth, illustrated in a simplified manner of Fig. 5, means that over time the average cost curves should be shifted in the way shown in Fig 5b. In such a situation, the maximum revenue may not necessarily be at the maximum value of the performance index. It may be for some products, therefore, that it makes more sense to design for less performance and less cost (Fig. 5c) [1,6]. It also means that cost minimization [7,8] (Fig 5d) becomes a much more attractive option in profit maximization than it used to be in the past.

The above simple consideration leads to an important conclusion: it is likely that with the advent of submicron technologies, the profit maximization of an IC operation requires careful analysis of the cost-price-performance trade-off. Such an analysis may produce results calling for less expensive manufacturing rather than higher performance. Hence, the most general objective for **DFM should be profit maximization achieved via optimization of IC cost-performance tradeoffs**[1]**.**

Is such an optimization feasible right now? The answer is: "not really". The reason is lack of adequate models describing the curves in Figs. 3 and 5. Observe, however, that despite the lack of needed models the following observations should still hold true: *In the submicron era minimization of unit cost via design and manufacturing means will have a larger impact on the profit than it used to have in the past*. Also, *the maximization of the revenue stream can be achieved by delivering to the market a volume of new product as soon as possible*. Such a strategy should allow the producer to maximize the unit price for a period of time when no competition is present and when early adopters, who are willing to pay a premium price, constitute the bulk of the demand.

The above leads to the conclusion, that **DFM**, as can be practiced today, should focus on **maximization of manufacturing volume achievable for lowest possible cost and with marketing-department-given performance.**

But such a task is not simple either. To highlight all the essential elements of the above definition of DFM let us consider again the relationship depicted in Figs. 1 and 2. Observe that maximization of revenue can essentially be achieved by fabricating, as quickly as possible, the desired volume of ICs. This means that the allocated manufacturing capacity (Fig. 2a) must be used with maximum efficiency, i.e., with as high a wafer productivity as possible (see eq. 2 and Figs. 2b and 2c). Maximum wafer productivity, i.e., maximum number of working dies per wafer, can be achieved by a design which produces the best product of yield and the number of chips per wafer [2,6], and not the smallest die area[2]**.**

Hence **DFM**, i.e., "maximization of manufacturing volume achievable for lowest possible cost" **should provide a design which maximizes:**

a. Wafer productivity, and

b. Rate of yield learning.

Such design objectives constitute necessary and feasible goals for submicron domain VLSI circuits. The remainder of this paper explains how such objectives can be achieved.

3. Yield

Due to space limitations the discussion of manufacturing yield must be limited in this paper to the presentation of only a few basic facts.

3.1. Yield loss mechanisms Yield loss occurs when there is an unacceptable mismatch between the expected and actual parameters of a fabrication process [11]. Such a mismatch may occur due to process disturbances and/or non-optimal design. These may cause either inadequate performance (e.g., excessive power consumption, too long delay) or functional failure.

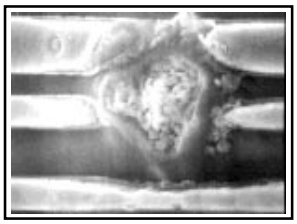

Figure 6. Example of a spot defect.

Typically inadequate performance is caused by a process-design mismatch, producing ICs with an excessive sensitivity to "global process variations". (They are called "global" because disturbances of this kind affect all fabricated ICs on a wafer [7,11].) Functional failures are due to "spot defects" which produce shorts or opens in the circuit's connectivity (Fig. 6). Since both mechanisms are exclusive, yield loss is often represented by the product $Y_{fnc}Y_{par}$, where Y_{fnc} is the functional yield associated with spot defects and Y_{par} is the parametric yield associated with global process. Both yield components change over time (see Fig. 7). At the beginning of the product life-cycle parametric yield loss is likely to dominate (period A1 and A2 in Fig. 7) [11].

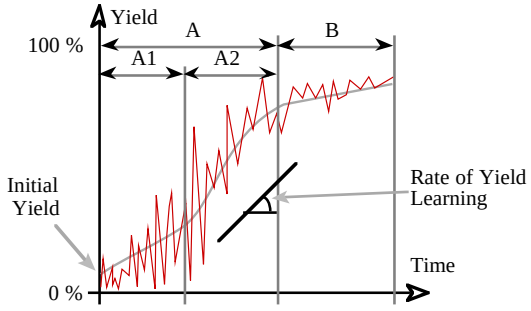

Figure 7. Yield as a function of time.

During this period, many fabricated chips do not work due to a design-process mismatch [11], which is corrected either via changes of process parameters or by IC re-design. Such a yield loss can also be seen as a result of poor DFM, leading to

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[1] For instance, yield improvement by a die per wafer in a modern high volyme manufacturing (7500 wafer starts a week) may result in $15 million of extra revenue per year! (Selling price per die = $40).

[2] It has been demonstarted with the actual yield data that yield can grow with die size [9,10]. This contradicts the typical assumptions about the yield-die size relationship used in a typical design paradigm.

insufficient process characterization, inadequate yield models or wrong strategic choices (too large die size, too ambitious performance goals, wrong process-design centering, etc.).

When initial yield difficulties are overcome, spot defect yield loss mechanisms become dominant. The level of yield loss is again determined by design attributes and process quality. The rate of yield increase (period A2) is a function of the efficiency of failure analysis which also depends on such product characteristics as the ease of detection of defects causing failure. (For instance, memories are the best defect monitors, allowing for fast defect localization.) In the last period of the product's life cycle, yield usually saturates at the level decided by the sensitivity of fabricated ICs to spot defects.

3.2. Yield loss in submicron era The key DFM-related characteristics of submicron technologies are: large number of manufacturing steps, very small feature size, large die area, large wafer size, 3-D nature of the interaction between elements of an IC, and low supply voltage, to name a few. These characteristics will not only intensify traditional yield loss mechanisms (e.g., process design miscentering due to a difficulty in maintaining process uniformity over a large area of a wafer) [1], but will also trigger new failure modes that are difficult to detect and control. The best example here would be data dependent and cross-talk based bridging faults which are due to coupling between densely packed segments of the interconnect [12]. All of the above will make maximization of initial yield and yield ramping much more time consuming and costly [1]. In addition, due to different functions served in the circuit by various elements of the interconnect and phenomena such as proximity effect (e.g., [13]), the concept and application of simple design rules will be inadequate.

3.3. DFM-related models IC design is a lengthy process with a long sequence of decisions affecting IC manufacturability. Many of these decisions, which have an impact on cost of manufacturing and IC performance, must be made long before important details of the design are known. (For instance, the number of metal layers or the minimum feature size are chosen in a subjective way at the beginning of the design cycle and sometimes before the chosen technology is fully developed.) Therefore, DFM needs a spectrum of models which can produce yield and then cost estimates at all stages of the design cycle. Below we present a small subset of such models.

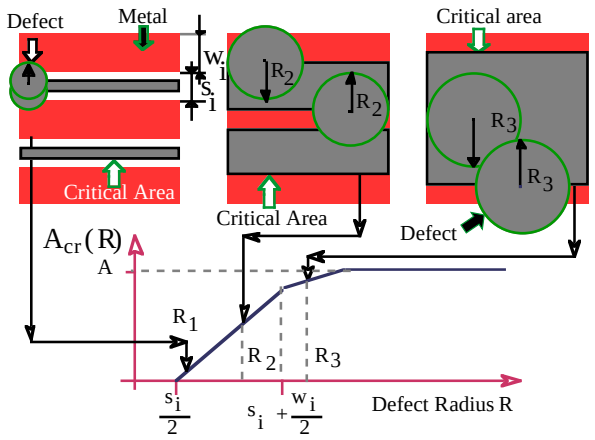

Figure 8. Concept of critical area function.

3.4. Yield models To explain the essence of the modeling strategy needed for DFM applications, let us assume that the defect is a contamination-generated spot (disk) of extra conducting, semiconducting or insulating material embedded in a layer of the IC during the manufacturing process [14,15,16]. Such a disk may (but does not have to) cause a fault (i.e., IC malfunction) and consequently yield loss. Whether a defect causes a fault or not depends on its size and location. Fig. 8 shows three segments of parallel metal lines and three groups of defects of increasing radius. Observe that spots of conducting material can cause a short between the non-equipotential lines only if their centers are located inside of a "critical area" [14,15,16,17]. The larger the defect, the larger the critical area (until it reaches the area of the entire die). This indicates that yield estimation must be based not only on the defect density but also based on the defect size distribution. One can show that the critical area function and the defect size distribution function can be used to compute yield [14] for a single layer using the following simple formula:

$$Y = exp\left[-\int_0^\infty A_{cr}(r)\ D(r)\ dr\right] \qquad (3)$$

where:

$A_{cr}(r)$ - is a critical area function of defect radius r;

$D(r)$ - is a defect size distribution.

Using eq. 3 one can also express yield due to shorts and opens for all IC layers [15]. The critical area for shorts and opens can be calculated using tools such as those described in [17,18,19].

It is also important to see that by increasing layout density one can affect the critical area function in the way shown in Fig. 9. Notice that more aggressive feature sizes shift the critical area function towards smaller defects but also decrease die size. The nature of the defect size distribution is such that there are more small defects than large defects. There are a number of functions which can be used to model a defect size distribution [15,20,21]. The most widely accepted -- due to its simplicity - is the function shown in Fig. 10 which decreases above a certain value, R_0, as R^{-p} where R is defect radius and p is a parameter [21,22].

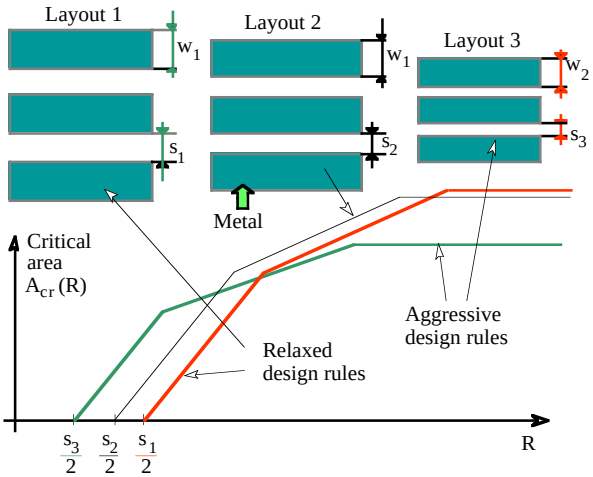

Figure 9. Critical area function for three different layouts.

Note that depending on the value of p the area below the product of functions $A_{cr}(r)$ and D(r) may grow or decrease when more aggressive (i.e., smaller) spacing is used [1,23].

Consequently, yield may decrease or increase when a new process (with smaller feature size) is applied.

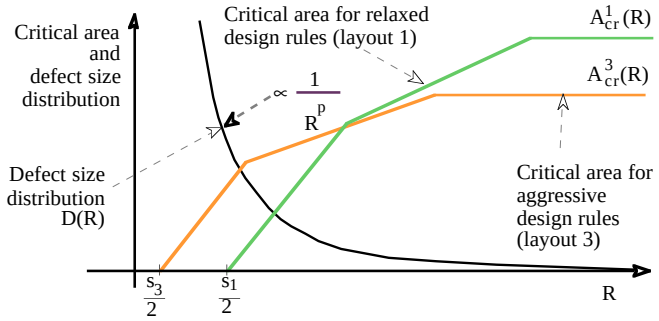

Figure. 10. Defect size distribution and critical area functions.

Pre-Layout Yield Modeling The above yield model in eq. 3 takes the critical area of the IC layers as input. But the critical area is not known until the latter stages of the design process, when the layout is complete. Unfortunately, it is often desirable to estimate yield in the earlier design stages to quickly assess the effects of design decisions on the IC manufacturability.

A model that predicts yield in the earlier stages of the design process is presented in [24]. This model takes as input a standard cell netlist and produces as output a yield estimate without performing placement and routing. This yield model has been successfully used to predict the interconnect yield of standard cell designs.

Fig. 11 shows the modeled metal1 yields of the interconnects of ten standard cell designs. The model yields were derived with two models, one is the model mentioned above, the other is the critical area model in eq. 3 [24].

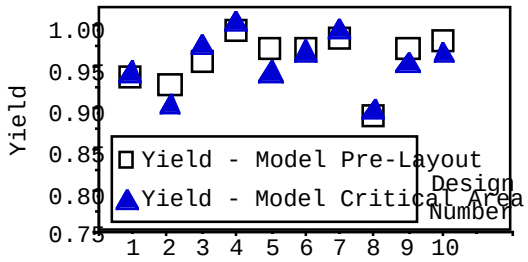

Figure. 11. Estimate of metal1 yield [24].

Design Density-Based Yield Model The critical area function of various IC layers are correlated to each other [9,10]. One can also demonstrate that they are correlated to other attributes of a circuit such as transistor density. Consequently, one can express yield as a function of design density. Two such models [9,10] have been postulated and verified with actual yield data. Note that transistor density can be estimated when the design style is decided for each functional block of an IC. In this way an estimate of the yield can be obtained in the early stages of the design process.

Yield Learning Modeling As indicated above, to perform cost-revenue trade-off studies it is important to model yield versus time curves and the resulting cost curves. Modeling the yield versus time curve has been attempted by several researchers [25,26], but not all have accounted for design-relevant IC attributes. Only the simulator Y4 (Yield Forecaster) [27,28,29] enables DFM-based trade-off studies.

Y4 has been built assuming that DFM-oriented modeling of yield learning should be described as a sequence of events starting with the introduction of particles (contamination), followed by the detection of defects and identification of their source, and concluding with eliminating the source of particles. It should also take into account:

1. The relationship between particles, defects and faults;
2. Ease of defect localization which in turn depends on:
   a. size, layer and type of defect,
   b. level of "diagnosability" of the IC design and,
   c. probability of occurrence of catastrophic defects;
3. Effectiveness of the corrective actions performed;
4. The timing of each of the events mentioned above;
5. Rate of wafer movement through the fabrication process.

4. DFM Trade-offs

In Sec. 2 general DFM objectives have been discussed. In this section a number of specific DFM trade-offs illustrating the considerations of Sec. 2 are given.

4.1. Physical Design Level DFM

Yield-based Routing Typically, channels are routed using minimum channel width as the main objective function. Such channels have very densely packed wires which adversely affect the critical areas for shorts, leading to a lower yield. Yield can be improved by two methods:

(a) Yield-oriented routing: A yield-based component must be added to the router's objective function. A variety of such functions have been described in the literature [30,31,32,33], and can be used effectively to increase yield. For example, one channel optimized for yield using a simple critical area estimator to guide routing is shown in Fig. 12 (see [31]).

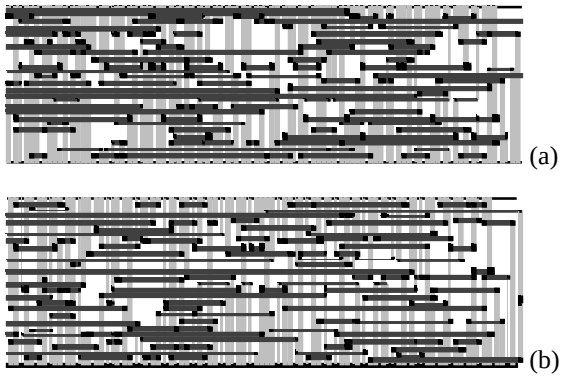

Figure. 12. Channel optimized (a) for minimum area, and (b) for yield [31].

(b) Yield-oriented post-processing: Horizontal wires in a routed channel can be swapped with one another (with the vertical wires adjusted accordingly) in such a way as to minimize the critical areas for all routing layers. This can be done using, for example, a simple simulated annealing-based algorithm.

Observability-based Routing. In some designs, high defect observability, driven by the need for rapid yield learning, is the main focus instead of yield maximization. In such a case one wants to route the channel such that every modeled fault that is hard to detect has a very low probability of occurrence [31,34].

This can be achieved by including a testability-based objective function in the router's objective function. An

example of a channel (same channel as in Fig. 12a) routed for bridging defect observability is shown in Fig.13 [31].

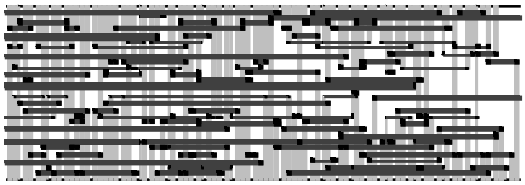

Figure. 13. Channel in Fig. 12a optimized for bridging defect observability [31].

Layout Compaction/Decompaction Once a complete layout is obtained, compaction/decompaction techniques can be used to minimize the cost of a working die [35]. Compaction leads to a smaller die (higher number of die per wafer) but may lead to lower yield. Decompaction has the opposite effect. There exists, therefore, an optimum point in terms of cost minimization.

Another application of decompaction is in the reduction of proximity effects [13]. An example of a software which can be adapted to perform this function has been given in [36].

Antenna Effect-Oriented Design In submicron technologies, a problem arises due to charging by plasma of polysilicon/metal conductors which are connected during manufacturing only to the gate. This can happen during the etching of poly, contact or metal layers. These charges can lead to gate oxide breakdown and consequently to yield loss [37]. The magnitude of the charge buildup depends on the geometry of the floating conductors [38] (or so-called antennas). One can devise a design strategy which limits the antenna effect [38,39].

4.2 Cell Library Design Level DFM Standard cells are typically designed with a minimum area design objective. However, cells can also be designed for yield, using simulators such as CODEF [40,41]. For example, by simulating the process flow and contamination statistics, two layouts for a 2-metal CMOS nand gate were found (after 1000 CODEF simulations each) to have "kill-ratios" of 0.31 and 0.29. (The kill ratio is the probability, i.e., fraction of simulations, that the cell fails in the presence of a contamination.)

4.3 Logic Synthesis for Manufacturability Logic synthesis tools can well benefit from incorporating design for manufacturability models into their objective functions. However, little has been done in this area other than incorporating die area estimation models. For example, during the FSM synthesis stage of logic synthesis, the resource allocation of registers and arithmetic logic units directly affect the number of cells. In addition, the "parallization" or pipelining of a design affects its interconnectivity. Both affect area and critical area and hence yield and manufacturability. Unfortunately, while a number of prediction tools are available to estimate area and delay from an RTL data flow, little work has been done on yield estimation.

Models do exist, which can be used for the prediction of area and yield during the logic decomposition and multilevel logic minimization stages of a logic synthesis tool. These models take as input a gate-level netlist and produce as output an estimate of area [42,43] and yield [24].

4.4 High Level Design Trade-offs

Choice of Number of Metal Layers The number of metal layers with which to design an IC imposes several tradeoffs on the manufacturability of an IC [2]. On the one hand additional layers lead to smaller die areas. Smaller dies imply fewer defects per layer, as well as more dies per wafer. However, extra layers also imply additional yield loss. Depending on the defect densities of these layers, extra yield loss can offset any gains acquired from the reduction in area. Also, extra layers imply added processing steps and hence extra wafer cost.

To demonstrate the tradeoffs imposed by an extra layer of metal, two layouts were generated using commercial tools for two industrial designs. The first layout was generated with 2 layers of metal; the second with 3 layers. The difference in area was 28% for the first design, and 43% for the second design.

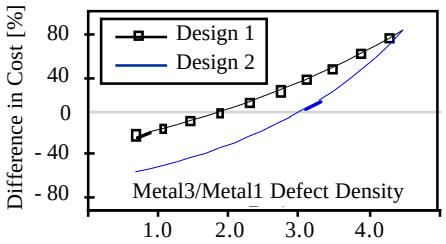

Figure. 14. Impact of Metal3 application on die cost.

Fig. 14 shows that for design 1, the extra layer of metal is cost effective if the defect density in the metal3 layer is less than 2 times that of the metal1 layer. For design 2, which benefits from a larger reduction in area than design 1, the 3 metal layer implementation is cost effective as long as the defect density in the metal3 layer is less than 3 times that of the metal1 layer.

Choice of Feature Size or Scaling Factor IC layouts obtained using the feature size given by the design rules may not always be the best choice in terms of yield and productivity. Fig. 15 shows a contour map, with cost computed per transistor in terms of the feature size and number of transistor in the circuit. As one can see, for different number of transistors there is a different optimum feature size from a cost per transistor perspective [1].

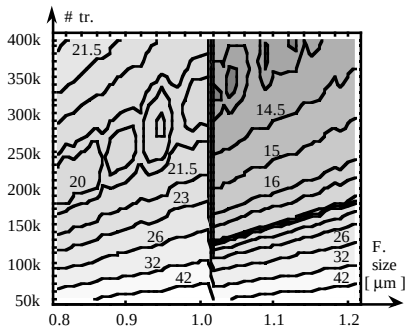

Figure. 15. Cost per transistor as a function of feature size.

Choice of Design Style A given schematic can be implemented in a variety of design styles - custom, standard cell, or gate array. Typically, this decision is based on a trade-off between time-to-market and performance. For example, designs are implemented quickly in semi-custom to capture the market, and are then migrated to full custom for higher

performance and smaller die area. It is assumed a smaller die area also leads to better yield, thereby lowering costs.

However, such an evaluation can lead to errors. As indicated by the transistor density-based yield model [9,10] in Sec. 3, the higher the design density, the lower the yield. There exists a significant difference in design densities between custom and semi-custom styles. For an industrial design house, densities (in transistors per square) were 1/121, 1/248, and 1/92.6 for custom, standard cells and SRAMs [6]. Thus, in spite of a lower die area, custom designs may actually have lower yields and hence *fewer* working dies per wafer. The resulting rise in cost may be more that the anticipated rise in profits due to higher performance. It is important, therefore, to properly evaluate design migration costs.

Design for Defect Diagnosability The yield learning rate achievable with a given product dependents on the ease with which defective ICs are diagnosable for the probable cause of failure. From a product design perspective, diagnosability can be improved in several ways. The obvious method of achieving this is to improve the observability of the circuit using techniques such as scan chains, internal test points and extra circuitry to make internal nodes accessible. In particular, for products with internal memory structures (cache, ROM, etc.), one can make these accessible for off-chip testing. Better observability can also be achieved by appropriately designing diagnostic testing procedures, and exploiting the circuit structure to obtain tighter bounds on the defect location [44,45,46]. Each of these methods will, however, have a different impact on the diagnosability of faulty ICs and cost.

The impact of diagnosability of defects can be well illustrated using Y4-based simulation experiments [29]. A factory producing a 0.6µm 3-metal CMOS IC was simulated for 75 weeks period and for a spectrum of diagnosability conditions. The results are shown in Table 1, where each column is obtained by setting As - the mean area of search for defects - at a certain value. Lower values of As indicate higher diagnosablity. One can see that if one is able to increase the localizability of defects by properly designing a circuit, both productivity and cost of die can be improved dramatically. Details of the above simulation can be found in [28].

	mean As = 0.08	mean As = 0.16	mean As = 0.32	mean As = 0.40
No. of good die (x 10^6)	2.017	2.086	1.758	1.364
Cost of good die ($)	95	91	108	139
Failure analysis cost (%)	6.08	5.54	5.87	5.23

Table 1. Cost impact of diagnosability of a product.

5. DFM Roadmap

As indicated several times in this paper, DFM should be a very important element of any IC design paradigm. At the same time, it should also be evident that many components of the DFM arena are still missing or in their infancy. Fig. 16 attempts to summarize the overall DFM field and suggests several tasks that need to be addressed.

The first set of tasks includes the following:

Identification of Market Conditions enabling quantitative assessment of price-performance trade-offs of the products to be designed.

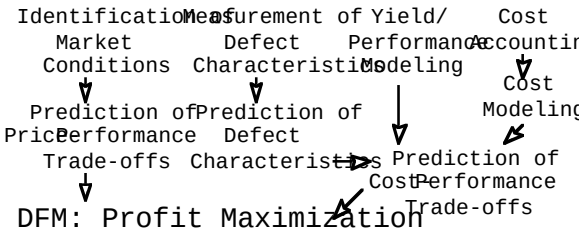

Figure 16. DFM Roadmap.

Measurement of Defect Characteristics for extracting defect density and size distributions for each critical layer of fabricated devices. These can be done via test structures (e.g., [22]) or by defect monitoring equipment (e.g., [47]).

Cost Accounting which allows monitoring of design and manufacturing cost. The granularity of accounting must be such that one can easily identify DFM trade-offs (e.g., estimating cost of each metal layer, or design cost for performance maximization).

Yield and Performance Modeling which allows the estimation of die area, yield and key performance metrics at all stages of design abstraction (e.g., models published in [6]).

The second set of tasks (2nd layer in Fig. 16) involves forecasting time domain trends of price-performance and cost-performance relationships. (The first step is the prediction of yield learning curves as implemented in Y4.)

When all of the above tasks are addressed adequately, true DFM will be feasible. Of course, before one can reach such a state, various DFM tasks (as described in Sec. 4) should be solved.

6. Conclusions

This tutorial has attempted to describe the current status and a vision for the future of DFM. It was illustrated through several examples that a design aiming for the smallest die size for a given technology (i.e., set of design rules) may not be the best strategy for the submicron era. Instead, the understanding and modeling of phenomenon affecting IC yield lies at the heart of DFM. In addition, manufacturing yield - expressed in terms of design attributes, process conditions and time - was shown to be a key component of DFM trade-off strategies. Profit maximization was also indicated as the ultimate DFM objective. Finally, it has been suggested that in order to fully implement the DFM vision, a number of problems must be solved. The stress must be on forecasting cost and performance characteristics of products to be designed and manufactured.

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