Metrology for Analog Module Testing Using Analog Testability Bus

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Abstract

In this paper, we propose a method to generate high quality test waveform on chip to avoid the parasitic effects in an analog testability bus test environment. For the test response analysis, we derive an extraction methodology to remove the parasitic effects and obtain the intrinsic response of the CUT. The test results show that the algorithm is robust such that the intrinsic responses remain the same regardless of the small variation in the test waveforms. With the concept of intrinsic responses, we are able to use a single library for the testing and diagnosis of multiple instantiation of an analog module.

1 Introduction

After the standardization of IEEE std. 1149.1 [1] and 1149.5 [2], the analog testability bus becomes an emergent task before completing the *design for testability* (DFT) for electronic testing. The structure and metrology of the analog testability bus proposed in [3][4] are the basis for the deliberations by the IEEE P1149.4 Working Group. From the structure point of view, the bus provides structural DFT for the testing of interconnects, discrete analog components, and analog functions within ICs. From the metrology point of view, it is mainly focused on the testing of discrete analog components and interconnects [3][5]. Here we would like to discuss the metrology for the testing of internal analog functions. Before our methodology is discussed, we would like to survey the analog testability bus proposed in [3], discuss the advantages and disadvantages for internal function testing, and study some major issues in board level testing.

The analog testability bus is a super set of IEEE Std. 1149.1. In addition to the four mandated digital pins for 1149.1 interface, it requires two analog testability buses, ABUS1 and ABUS2 and a switching network, as shown in Figure 1. With the buses, one can apply the stimulus through one bus and observe the responses from another bus. In the switching network there are five switches, namely, **V** (connection to a power rail), **G** (connection to ground), **A1** (connection to ABUS1), **A2** (connection to ABUS2), and **CD** (core disconnect). The switching networks are identical for each pin. Based on this structure, some proposed the use of single wire to minimize the overhead [5] and others modify the digital interface for the better integration with 1149.1 [6].

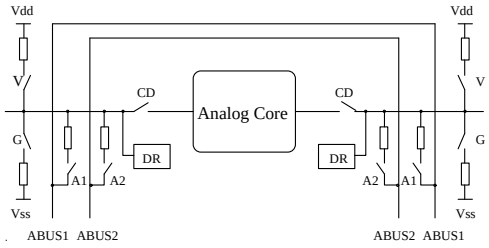

Figure 1: Analog Testability Bus [1]

With the bus structure, the major concern for analog testing is the large parasitic reactance, capacitance and inductance. For interconnect testing, such a parasitic reactance will not affect the DC testing of short and open faults. For discrete component testing, the mounted R, L, and C, in most case, have the time constant greater than the on-board wires. The exception occurs in very high frequency circuitry where wires are used to implement inductors and capacitors. Otherwise, the bandwidth of the bus is sufficient for discrete component testing [3, 5].

However, for the internal analog function testing, there are some difficulties. As we know, modern technologies are able to produce ICs with the performance exceed that of the interconnects. For instance, operational amplifiers with f_t over 100MHz are common. While, 100MHz PCBs require a significant design implementation efforts. For high speed circuits, the interconnects must be optimized in order to boost the overall speed. It is very unlikely that the analog testability buses are optimized as well. Note that, it is already a known fact that the scan clock is far slower than the system clock in serial scan DFT. Therefore, testing internal analog functions through testability buses will face the challenge of the limited bandwidth caused by the reactive parasitics. In Section 2, we will study the modeling of wires, vias, and pins briefly.

For internal module testing, another challenge is on the test data management. A chip can be placed in

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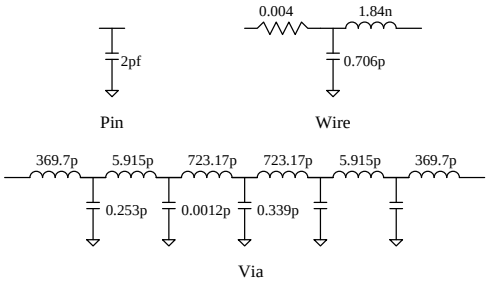

Figure 2: Interconnect Modeling

different boards and/or different locations of a board. With the large parasitics, the test inputs and response waveforms will be different from case to case. Therefore, one must build an individual library for each instantiation of the chip. This creates a significant overhead. Ideally, we need only one library for all the instantiations. Therefore, a test methodology which is capable of utilizing only one test library is desirable. Moreover, the parasitics of printed circuit boards vary a lot. If the test signal frequency is at the neighborhood of or higher than the wire cutoff frequency, the situation becomes very complicated. It may invalidate the test. Therefore, a mechanism to exclude the variation and obtain the intrinsic response is also desirable. Here, the *intrinsic response* is the response with ideal input signal and without the parasitic effect of the interconnect wires. In other words, it is the response when the chip is test alone.

In this paper, we would like to propose a method to exercise internal module testing in an analog testability bus test environment. We emphasize on the utilization of single test library and the removal of the parasitic effects. To achieve the goals, we have to face and solve the following challenges. The first one is the generation of quality test waveform in an analog testability bus test environment. The second one is the modeling and the measurement of the parasitic effects of analog buses. The third one is the exclusion of the parasitic effect in order to extract the intrinsic response as if the chip is tested alone. In the rest of this paper, the details of these issues are discussed as follows. In Section 2, the analog scan bus modeling and intrinsic response extraction method are discussed. In Section 3, the test methodology is studied in detail. In Section 4, some test results are presented to show the feasibility of the method. Finally, in Section 5, the conclusions are given.

2 Interconnect Modeling and Response Extraction

Testing an analog module through analog testability bus requires not only the knowledge about the CUT and the bus but also the technique to analyze the observed response waveform to exclude the parasitics. In this section, we will study the modeling of analog testability bus, show the circuit under test, and present the iterative deconvolution for intrinsic response extraction.

Testability Bus Modeling

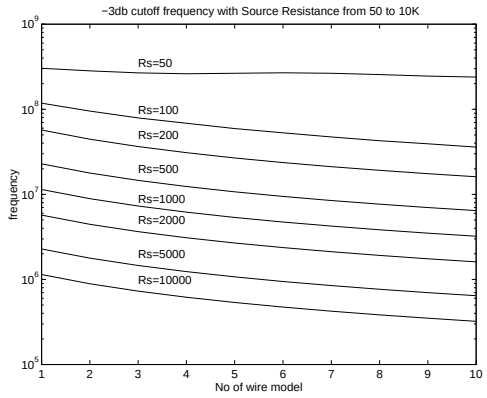

Figure 3: Wire's 3dB Frequency as Function of Number of Wire Segment

Interconnect modeling is a specialized topic in computer aided design. It study how to model wires, vias, and pins in order to produce the simulation results that are as close to the real circuit behavior as possible. Since our concern is to include the parasitics of interconnects into consideration, we borrow the results from [7] to build the SPICE model for simulation. Here, the models for wires, pins, and vias are shown in Figure 2 [7]. To simplify the cases, we assume that the analog testability buses are separated into several wire segments. Each segment consists a wire of 2cm long, a pin, and a via. Of course, a physical wire segment may differ a lot. Figure 3 shows the 3dB frequency of the wire in terms of number of wire segments. Different curves represent the responses under different source resistances. The measurement is based on the loading of $10M\Omega$ and $10pF$, a typical loading for a probe or instrument. In the rest of the paper, we assume the testability buses from board boundary to the circuit under test consist of ten wire segments. From Figure3, the bandwidth is from 3 MHz to 30 MHz for the source resistance between $1K\Omega$ and 100Ω.

Circuit Under Test

Circuit under test is a CMOS operational amplifier, as shown in Figure 4, in the inverted negative feedback configuration. The f_t of the amplifier is $17MHz$. The testability buses, connected to the input and output of the OP, contain ten wire segments each. All the test data are obtained by SPICE simulation. With such a setup, we include not only the nonlinearity of the transistors in the OP Amp but also the parasitic effects of the switching devices and testability buses in the DFT construct.

Intrinsic Response Extraction

For the intrinsic response extraction, we utilize the iterative deconvolution technique proposed in [9] to extract the impulse response of a module from a multimodule configuration. The basic concept is as follows. For the system $H(s)$ and the parasitics $P(s)$ shown in Figure 5, the time domain and frequency domain representation are as follows.

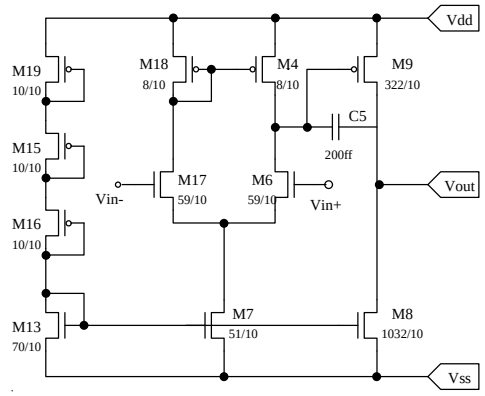

Figure 4: CUT - A CMOS Operational Amplifier

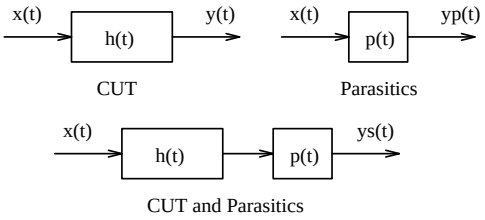

Figure 5: Serial System Modeling of CUT and Parasitics

Time Domain	S Domain
$y(t) = x(t) * h(t)$	$Y(s) = X(s) \cdot H(s)$
$y_p(t) = x(t) * p(t)$	$Y_p(s) = X(s) \cdot P(s)$
$y_s(t) = x(t) * p(t) * h(t)$	$Y_p(s) = X(s) \cdot P(s) \cdot H(s)$

$y(t)$ is the intrinsic response of the circuit under test when it is tested with ideal input and without parasitic effects. $y_p(t)$ is the response of parasitic effects and $y_s(t)$, the response of the CUT with parasitic effects.

If $y_p(t)$ and $y_s(t)$ are know, by mathematical operation in S-Domain, the impulse response $H(s)$ of the CUT can be extracted by

$$H(s) = \frac{Y_s(s)}{Y_p(s)}.$$

The direct division in S-domain will encounter the divide-by-0 problem. So, [9] proposes the use of iterative deconvolution to obtain the inverse of a Laplace function. For this, a *compensating filter function* $C(s)$ is defined as follows to replace the direct division.

$$C(s) = \frac{Y^*(s)}{|Y(s)|^2 + \lambda}$$

Here, an iterative algorithm is used to find the optimal λ^* that yields the best estimation of the signal. Bennia and Riad partition the transfer function into several frequency intervals based on the degree of information in each interval. In the successive step, they use the minimum root-mean-square error criterion to find λ^*.

Such a method has the following the advantage of input signal independent. By this we mean, the extracted responses remain the same despite there are small variations in the input signals. Note that in the real test environment, it is very difficult to or produce exactly the same signals exactly every time. In [8], we have used the technique to extracted faults for functional level analog module described as S-domain equations. The challenge here is to apply such a linear technique on the results by SPICE simulation. Note that, transistors in SPICE are modeled nonlinearly.

In this section, we have presented the wire model, circuit under test, and the intrinsic response extraction method. In the next section, we will present a methodology for test pattern application and intrinsic response extraction.

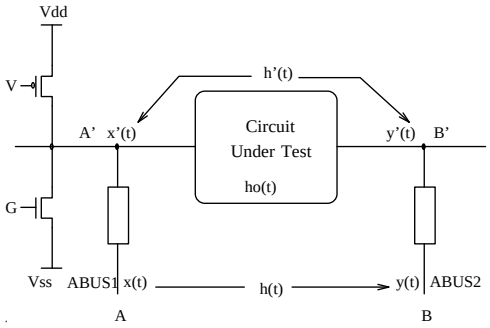

Figure 6: Test Environment

3 Test Methodology

In this section, we will discuss the generation of test waveforms in the analog testability bus test environment, derive a methodology to remove parasitic effects and extract intrinsic response, and present the experimental results for systems with and without testability bus for comparison.

Test Waveform Generation

Figure 6 shows the test environment. The circuit under test is the operational amplifier presented in the previous section. For the analog scan cells, only the related switches are shown. Here we assume that ABus1 and ABus2 are identical such that, the wires from board's boundaries A and B to chip's pins A' and B' have the same impulse response $p(t)$. The reasons are as follows. Structurally, the two buses are symmetrical with the same connections to the chips. Physically, the wires are likely to run in parallel to minimize the layout space and obtain the balanced performance. In this paper, both wire, ABus1 and ABus2, contains ten wire segments.

In the proposed analog bus [3], the analog pins are connected to V_{dd} and V_{ss} through V and G switches. The test signals can be produced by switching V and G switches on and off in turn to produce a pulse at A'. As a result, we can utilize the pulse as a test signal for the step response of the circuit under test. Since the MOS transistor switches are connected to V_{dd} and V_{ss}, the test waveform will have a full swing from V_{ss} to V_{dd}. This may cause the CUT to saturate. Nevertheless, we can have V and G switches connected to a resistor voltage divider to control the input swing. Since the pulse is generated internally, it is immune from parasitic effects of the testability buses. How-

ever, the deviation of the switching devices and their drivers may result in different outputs even though the CUTs are identical. In the next subsection, we will discuss the technique on the exclusion of such a deviation and wire parasitics in order to extract the intrinsic responses.

Intrinsic Response Extraction

For the internal generated pulse at A', denoted $x'(t)$, we can observe it at A, denoted $x(t)$. The output response at B', $y'(t)$, can be observed at B, denoted $y(t)$. We can use the following equations to express their relationship.

$$x(t) = x'(t) * p(t)$$

$$y(t) = x'(t) * h(t) * p(t)$$

By the deconvolution of $x(t)$ from $y(t)$, using the technique described in Section 2, we are able to obtain the impulse response $h(t)$ of the CUT. Then, we convolute the $h(t)$ with an ideal pulse ($u(t)$) to obtain the intrinsic response. The related equations are as follows.

$$H(s) = \frac{Y(s)}{X(s)}$$

$$y_o(t) = h(t) * u(t)$$

By this, we not only exclude the parasitic effects of $p(t)$ but also the deviation of the internally generated test signal $x'(t)$.

Figure 7 shows the extracted intrinsic responses without wire's parasitics, for comparison purposes. In other words, it is extracted from the signals measured at A' and B'. Figure 8 shows the responses with parasitics, extracted from A and B. Let's us study the one without parasitic effect first.

Figure 7, shows the the signals observed at A' $x'(t)$ in column 1, the signals observed at B' $y'(t)$ in column 2, and the extracted intrinsic responses $y'_o(t)$ in column 3. Row 1 shows the case with ideal V and G control signals, without delay and rise time. The rest rows show the results with the V and G control signals having delay (row 2 and 3) or rise time (row 4 and 5). Let's look at row 1 first. One may wonder why $y'_o(t)$ (row 3) is different from $y'(t)$ (row 2). The reason is as follows, $y'(t)$ is equal to $h(t) * x'(t)$, where $h'(t)$ is the extracted impulse response of the CUT from $x'(t)$ and $y'(t)$. While, $y'_o(t)$ is $h'(t) * u(t)$ where $u(t)$ is the ideal control signal that produces $x'(t)$. We do run a reverse operation to convolute $h'(t)$ and $x'(t)$. The results match that of $y'(t)$ exactly. So, we are sure that the deconvolution function correctly. After certain analysis, we conclude that the small ripple is caused by the DSP operation on the high frequency components in the ideal pulse. Such frequency components never show up in the rounded waveforms in $x'(t)$. Later in Section 4, we will show that such ripples do not affect the testing.

From the second row on, they are tests with different delay and rise time to emulate the behavior of a tester. Row 2 and 3 are the cases with delay of $1\mu s$ and $2\mu s$ respectively. Row 4 and 5 are the cases with rise time of $100ns$ and $200ns$ respectively. The $y'_o(t)$ in row 2 and 3 are identical to that of row 1. In other words, such an extraction method allows offsets in the sampling the waveforms. The $y'_o(t)$ in row 4 and 5 are a little different from that of row 1.

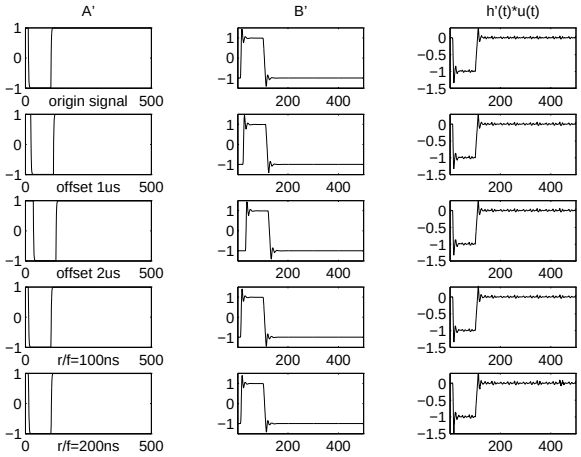

Figure 7: Fault-Free Intrinsic Response Extraction Without Wire's Parasitics

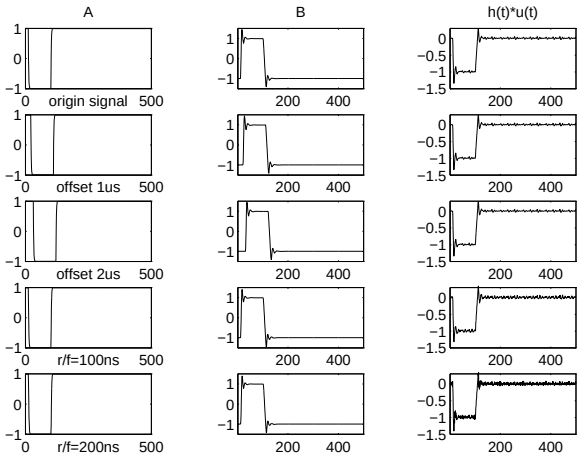

Figure 8: Fault-Free Intrinsic Response Extraction With Wire's Parasitics

Figure 8 shows the responses with the parasitic effects of wires of ten segments. $x(t)$ are shown in column 1, $y(t)$ in column 2, and the extracted intrinsic response $y_o(t)$ ($h(t) * u(t)$) in column 3. Figure 8 is arranged in the same way as Figure 7. As one can see, the $y_o(t)$ of different delays (row 2 and 3) do not only identical to that of row 1 but also the row 1 of Figure 7. Again, $y_o(t)$ of row 4 and 5 are different from that of row 1. They are also different from that of row 4 and 5 of Figure 7.

So far we have presented our test methodology and shown the test results on SPICE simulation data. As one can see, the cases with rise time in V and G control signals create all the problems. In the next section, we will presented our test results on faulty circuits using

the worse test inputs, with 100ns and 200ns rise time. We will introduce a stochastic filter to handle problem for these two cases.

4 Test Results on Faulty Circuits

In this section, we would like to present test results on the intrinsic response extraction for faulty circuits using the switch control signals with rise time of 100ns and 200ns. The faulty circuits are obtained by changing the parameters of certain transistors in the CUT. The major task here is to show that errors in the intrinsic responses are almost identical with and without parasitics.

As we have shown in the previous section, the inputs with rise time create many noise like jitter. In order to remove these jitter, we pass the signal through a stochastic filter called $\alpha\beta$ filter. It is a simplified version of Kalman filter often found in control systems for the removal of random noise. In the rest of this section, we will shows some results from Figure 9 to 14. All the figures are arranged in the following manner. The top four figures are the errors of intrinsic responses. In order words, the differences of the intrinsic responses of faulty and fault-free circuits. Here, $h'(t)*u(t)$ is the intrinsic response obtained from A' and B' without parasitic effects. $h(t) * u(t)$ is the intrinsic response obtained from A and B with parasitic effects. $h_o(t) * u(t)$ is the intrinsic response of fault-free circuit. In other words, $h_o(t)*u(t)$ is the one shown in the first row of Figure 7. Also shown are the standard deviation of the waveforms. As expected, the rise time does create some problems and creates some noise-like jitter. This make identification difficult regardless whatever error criterion being used, RMS or absolute. We can see this from the given standard deviation. The next two horizontal strips show the errors after they are filtered by $\alpha\beta$ filter. We put the errors with and without parasitic effects in the same strip for comparison.

From these figures, we have the following observations. First, the errors with and without parasitic effects are almost identical after filtering. This implies that we have successfully remove the parasitic effects. Of course, the jitter caused by DSP operation is also handled well. As a result, we are able to use one library, library of intrinsic responses, for testing and diagnosis. This significantly simplifies the test data management problem mentioned in Section 1. Second, the errors with 100ns and 200ns rise times look alike in most case. Here, we have demonstrated the robustness of the extraction algorithm. As a result, the requirement on the ATEs can be relaxed because our method can tolerate small deviation of test signals. Third, there are cases, such as Figure 14, that the $\alpha\beta$ filtering does not function satisfactorily. This tells us that we still have some room for improvement. Forth, the extracted errors of different faults look differently. This implies that we are able to use the extracted errors to build fault dictionary for diagnosis.

5 Conclusions

In this paper, we have proposed a test methodology for the testing of analog function in analog testability bus test environment. The test waveforms are generated on chip to avoid the large parasitic effects and produce a high quality pulse for testing. An iterative deconvolution technique has been derived to remove the parasitic effects of the buses and extract the intrinsic responses. To show the feasibility of the methodology, the test case is composed of a CMOS operational amplifier with f_t of 17MHz and two analog testability buses which are 20 cm long with ten pins and 10 vias. From the test results we have two major conclusions. First, the extraction algorithm is robust because it can tolerate small deviation of input waveforms. Such a property relax the constraint on test equipment. Second, the removal of parasitic effects make the use of single test library for the testing and diagnosis of multiple instantiations possible. As a result, the complexity of analog testing and test data management are reduced significantly.

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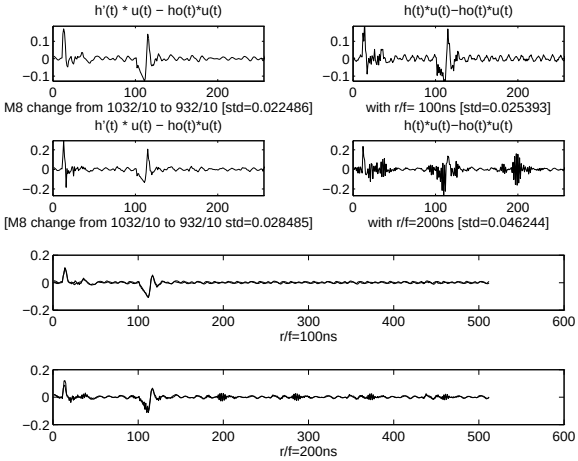

Figure 9: Test Results on Faulty Circuit 1

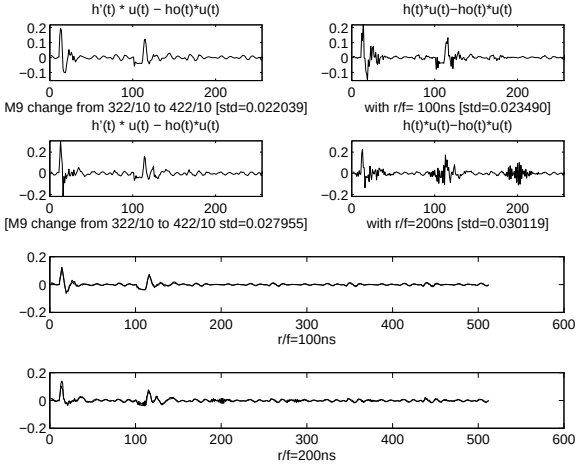

Figure 10: Test Results on Faulty Circuit 2

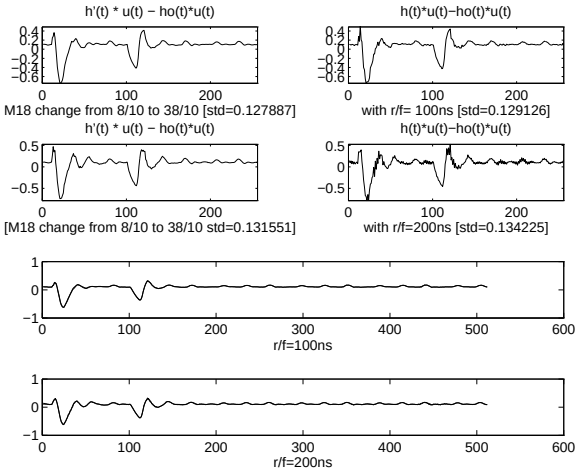

Figure 11: Test Results on Faulty Circuit 3

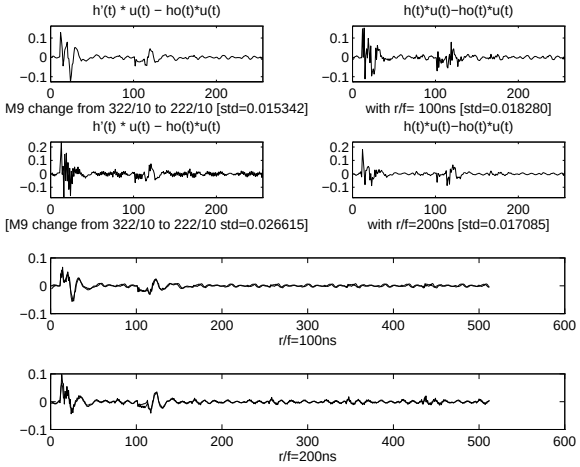

Figure 12: Test Results on Faulty Circuit 4

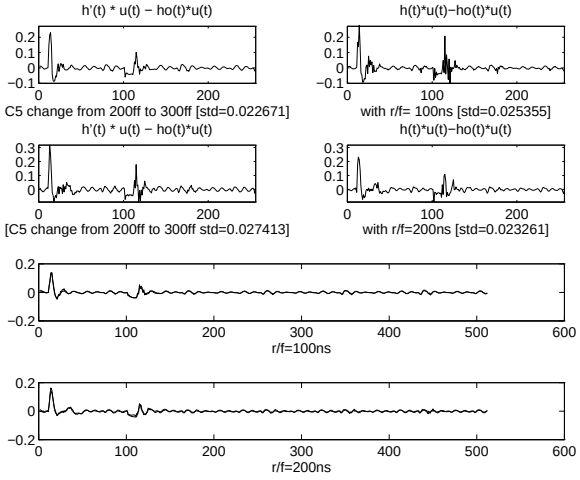

Figure 13: Test Results on Faulty Circuit 5

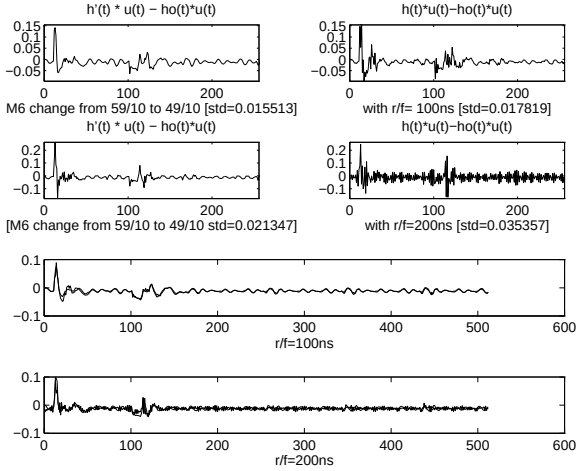

Figure 14: Test Results on Faulty Circuit 6