

Delay Fault Coverage: A Realistic Metric and an Estimation Technique for Distributed Path Delay Faults

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Abstract

In this paper, we propose a new and realistic definition of delay fault coverage, based on the percentage of fabricated faulty chips which can be detected as faulty by a given test set. This metric takes into account the probability distribution of delay fault sizes caused by fabrication process effects, as opposed to previously defined metrics which have been based primarily on the percentage of faults tested.

In addition to proposing a realistic delay fault coverage metric, we also present a computationally viable scheme for using this metric to estimate the coverage of any given test set for a class of path delay faults caused by distributed fabrication process variations. We use the results for the ISCAS'89 benchmark circuits to demonstrate wide discrepancies between distributed path delay fault coverage estimates for robust test sets obtained using our realistic definition, and the ones obtained by using the traditional notion of coverage as the percentage of paths tested.

1. Introduction

When a chip is fabricated, fabrication process effects cause *component* (i.e., gate and interconnect) delays to differ from the designer-specified values. This necessitates testing the fabricated chip for the presence of *delay faults*. If a fabricated chip passes a set of delay tests, the confidence one has in the absence of delay faults in the chip is a measure of the effectiveness of the test set. Previous research in delay fault testing [5][7][8] has quantified this notion in terms of the percentage of all possible delay faults which can be detected by the test set. This quantification has been used as a measure of the *delay fault coverage* of the test set, and has evolved from the definition of fault coverage for functional failures (e.g., stuck-at fault coverage), where the coverage of a test set is defined as the percentage of the total number of faults detectable by the

test set.

In the literature, delay faults have been broadly categorized into gate delay faults and path delay faults. For a particular case of the gate delay fault model, called the *transition fault model* [15], probabilistic measures to estimate the transition fault coverage as the percentage of faults which are detectable have been proposed [16][17]. For a more general case of the *gate delay fault model*, the size of the delay fault at a node needs to be considered to determine if the fault is detectable. The quality of a test set has been defined [18] in terms of how close the *actually detected* minimum delay fault sizes are to the respective circuit slacks at the faulty nodes (For a fault, the minimum delay fault size *possibly detectable* is the slack at that node). This is a more realistic metric of the gate delay fault coverage of a test set than simply the percentage of delay faults tested by the test set. However, the test quality metric still does not take into account the probability distribution of the delay fault sizes (which is a consequence of the fabrication process). The probability density function of the gate delay fault sizes has been incorporated in the statistical delay fault coverage metric derived in [20]. However, the metric is limited in scope to only single, localized gate delay faults along a path. Also, evaluating this metric is computationally expensive since the longest sensitizable path passing through the fault site has to be determined for each test of a given test set and for each gate delay fault site through which the test sensitizes a path. Lastly, no results for gate delay fault coverage using this metric have been presented.

As opposed to gate delay faults, *path delay faults*, as introduced in [4], deal with propagation delays along one or more paths exceeding the timing constraint. Most path delay fault test vector generators in the literature attempt to generate robust [5][6] and validatable non-robust tests [9] for paths. In these cases, the delay fault coverage of the resulting test set is determined as the percentage of paths which are testable in this manner, i.e., for a robust (validatable non-robust) test set, coverage = No. of robust (validatable non-robust) paths / total no. of paths. The same coverage metric is used in a probabilistic path delay fault

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coverage estimator [16] for robust and non-robust tests. Higher coverage estimates can be attained if *redundant paths* are not considered while counting the total number of paths in the circuit. It is shown in [10] that up to 81% of the paths may be redundant in the ISCAS'85 benchmark circuits. Eliminating *robust dependent* (RD) paths [11] also gives higher coverage numbers. For one of the MCNC benchmark circuits, it is shown [11] that the coverage estimate for the robust test set goes up from 1% to 21% upon eliminating the RD set while counting the total number of paths.

Since all these metrics of path delay fault coverage ignore delay fault sizes, the coverage value obtained is not realistic. This is because, depending on the slack of a path and the sensitivity of delays of the components lying along the path to fabrication process disturbances [3], the likelihood of each path delay exceeding the timing constraint is different. These fabrication process effects must be incorporated into the metric for coverage of a delay fault test set. Moreover, current path delay fault coverage metrics, based on the percentage of tested paths, handle test sets for only singly RV-testable path delay faults, i.e., path delay faults which are singly robustly testable or singly validatable non-robustly testable. These metrics suffer from many drawbacks. Firstly, an RV-test set may also detect delay faults on other non-RV-testable paths. This may happen when a non-RV-testable path gets sensitized for some component delay value combination where there is no fault on the RV-testable paths or the faults on the RV-testable paths are masked by the ones on the non-RV-testable paths. If this situation occurs only for certain component delay value combinations, the coverage metric based solely on the percentage of paths tested is incapable of handling such a case. Secondly, a test for a path which is not RV-testable may detect the path delay fault only under certain component delay conditions [13]. This case also cannot be handled by existing path delay fault coverage measures. Thirdly, the existence of multi path delay faults that cannot be tested individually has been shown [12]. Multi path delay faults, some of which may not be RV-testable, also cannot be handled by current path delay fault coverage metrics.

In this paper, we propose a realistic delay fault coverage metric that is based on the actual percentage of *faulty* chips that can be *detected as faulty* by the test set. This metric takes into account the delay fault size distributions as caused by the fabrication process, and is model-independent, i.e., equally applicable to both the gate and path delay fault model. Moreover, the metric is not limited in scope to single delay faults. Also, it can handle delay faults which are detected only for certain component delay value combinations.

We also present an estimation strategy which uses our

metric to determine the coverage of a given test set for path delay faults caused by *distributed* fabrication process effects. We term path delay faults caused by such distributed effects as *distributed path delay faults*. Here, the fault is assumed not to be localized at any one component - component delays vary due to the effect of the fabrication process in a correlated manner. The cumulative sum of excess component delays along one or more paths results in delay faults. This situation could arise in spite of the fact that each circuit component meets its individual delay specifications - because of correlation between component delays due to similar fabrication process effects, the sum of these delays along paths might violate a timing constraint. The previously mentioned gate delay fault modeling methodologies, with the fault lumped at a fault site, cannot handle correlated excess delays distributed over the chip components caused by distributed fabrication process effects. Furthermore, testing a circuit for distributed path delay faults is not a simple task (using a ring oscillator, for example) because different paths have different sensitivities to distributed fabrication process effects. This is due to two reasons - firstly, paths which have very little slack are more susceptible to delay faults than ones with greater slack, and secondly, the component delay variations due to distributed fabrication process effects, though correlated, are not the same [3]. Faults due to distributed fabrication process effects occur frequently in a new generation of process/product technology, therefore a distributed path delay fault model is a realistic one. In a mature fabrication process, localized defects which result in local delay faults are more common. A test set with good distributed path delay fault coverage will cover a majority of sensitizable paths which have small slack and whose delays are sensitive to fabrication process variations. Since sensitizable paths with small slack detect local delay faults very effectively, such a test set will also have good delay fault coverage in the presence of local delay faults. Thus, to certain extent, our coverage estimate under a distributed path delay fault model indicates the quality of a test set even in a scenario where delay faults are primarily caused by localized defects.

Section 2 motivates and explains our delay fault coverage metric, and also describes the problem of determining the coverage of a given test set for distributed path delay faults. Section 3 describes how we build component delay functions which model distributed path delay faults caused by distributed fabrication process effects. The coverage estimation approach itself is presented in Section 4. Section 5 describes experiments run on benchmark circuits, and makes some observations on the results obtained. Finally, Section 6 presents our conclusions.

2. Problem description

2.1. The coverage metric

A more realistic, statistical metric for delay fault test coverage of a given test set, test, is defined in terms of the probability that if there is a delay fault in a fabricated chip, the test set will detect it. More precisely,

statistical coverage(test) = $100 \times \text{Probability}(\text{test detects delay fault} \mid \text{fabricated chip has a delay fault})$.

This metric is elaborated on in the following discussion. Consider a circuit with n component delays $\Delta_0, \Delta_1, \dots, \Delta_{n-1}$. The vector of component delays $\underline{\Delta} = [\Delta_0, \Delta_1, \dots, \Delta_{n-1}]$, which is a set of random variables, can be expressed as a joint probability density function (jpdf), $f(\underline{\Delta})$, which is a consequence of the fabrication process and the type of fabrication process effects incorporated in the component delay model. Component delay models which reflect local fabrication process effects can be handled by a gate delay fault model. Distributed fabrication process effects, on the other hand, may cause incremental excess gate delays which add up along some paths to produce incorrect circuit timing behavior. This is beyond the scope of a gate delay fault model, but can be handled by a path delay fault model. In any case, any kind of fabrication process effect can theoretically be reflected in the jpdf, $f(\underline{\Delta})$. For the sake of illustration, consider a hypothetical case of a 2-dimensional component delay space $[\Delta_0, \Delta_1]$, shown in Figure 1.

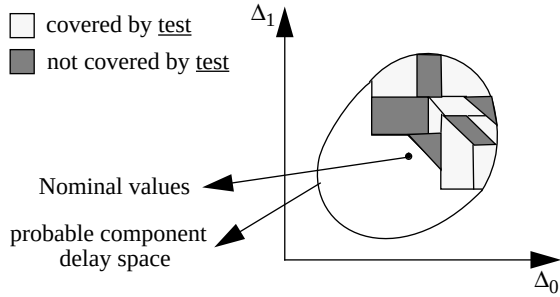


Figure 1. Coverage w.r.t delay space covered.

The space of probable component delay value combinations is represented by the bounded region, which is a given *level set*¹ of $f(\underline{\Delta})$. Within this space, the region representing those component delay value combinations for which the circuit will exhibit a delay greater than a pre-specified constraint T (say, the system clock period) is shown shaded. A path delay fault which is not RV-testable may have component delay dependent tests. In such a

case, multiple tests might be required to test a path in the entire space of probable component delay value combinations [13], where each test tests the path for a set of component delay value combinations. This is represented in the figure by dividing the shaded region into sub-regions, each of which corresponds to those component delay value combinations for which a test detects a single or multi path delay fault. Now, say that the tests in test only cover a few of these sub-regions. In the figure, these sub-regions are lightly shaded. The sub-regions not covered by the test set are shown shaded darker. The probability that a

fabricated chip has a delay fault is equal to $\int_{\mathbf{R}} f(\underline{\Delta}) d\underline{\Delta}$,

where the volume integral (for an n -dimensional component delay space) is taken over $\mathbf{R}$, the region where the chip has a delay fault, i.e., over all the shaded regions in the figure. The probability that the chip has a delay fault and the delay fault is detected by the test set is equal

to $\int_{\mathbf{R}_1} f(\underline{\Delta}) d\underline{\Delta}$, where the volume integral is taken over

$\mathbf{R}_1$, the sub-regions covered by test i.e., over the lightly shaded regions in the figure. The ratio of the two probabilities is the conditional probability $\text{Prob}(\text{test detects delay fault} \mid \text{fabricated chip has a delay fault})$. This multiplied by 100 gives the statistical delay fault coverage of test, which is the percentage of fabricated chips with delay faults that can be detected as faulty by applying the given test set.

2.2. Distributed path delay fault coverage

Our proposed metric for the delay fault coverage of a test set is general enough to be applicable to any delay fault model. However, the definition, by itself, does not suggest any scheme to determine the coverage of a given test set under a given delay fault model. In the remainder of the paper, we present a computationally viable strategy that uses our realistic metric to determine delay fault coverage under a restricted path delay fault model where path delay faults are caused by distributed fabrication process effects. We have previously called such a model the distributed path delay fault model. Although we do not consider delay faults caused by localized defects, our statistical coverage metric is applicable to such faults as well.

In the preceding sub-section, we have introduced our statistical delay fault coverage metric using the component delay space. For determining the coverage of a given test set for distributed path delay faults, we prefer to use the set of variables which represent variations in the fabrication process parameters, e.g., variations in transistor channel

1. A level set of a jpdf is the region of random variable value combinations (in this case, component delay value combinations) for which the jpdf is greater (or lesser) than some value.

width, channel length, oxide thickness, surface doping, mobility etc. By using this fabrication process parameter variation space, we eliminate the need to obtain the jpdf of the component delays, $f(\Delta)$, from the jpdf of the fabrication process parameter variations, $f(\mathbf{p})$, and the component delay functions, $\Delta = \Delta(\delta_{input}, C_{out}, \mathbf{p})$, where δ_{input} represents input transition time, and C_{out} represents output load capacitance. We use our metric for delay fault coverage and express it in terms of the fabrication process parameter variation space covered. Figure 2 shows a hypothetical

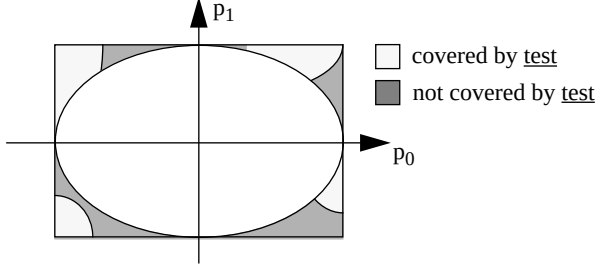


Figure 2. Coverage in terms of fabrication process parameter space covered.

2-dimensional example with variables $\mathbf{p} = [p_0, p_1]$ representing independent variations of two fabrication process parameters. The bounded region represents the space of probable fabrication process variations, as determined by some $\pm N$ -sigma variation of the jpdf $f(\mathbf{p})$ about its mean. The unshaded region represents those parameter variation combinations for which the circuit delay satisfies a pre-specified timing constraint. The lightly shaded regions represent the fabrication process parameter variation combinations for which there is a delay fault in the fabricated chip which is detectable by the given test set, test. Using the joint probability density function of $\mathbf{p}$, $f(\mathbf{p})$, the probability of this occurrence is equal to $\int_{\text{shaded}} f(\mathbf{p}) \cdot d\mathbf{p}$, integrated over the lightly shaded regions. Likewise, the probability of a fabricated chip having a delay fault is equal to $\int_{\text{unshaded}} f(\mathbf{p}) \cdot d\mathbf{p}$, integrated over all the shaded regions. The ratio of the two probabilities, when multiplied by 100, gives the percentage of actually fabricated faulty chips which are detectable as faulty by the test set. This is the coverage of the test set for distributed path delay faults, as defined by our metric.

3. Assumptions

3.1. Circuit operation

We perform our analysis for combinational circuits embedded in a synchronous system. This implies that each test vector is applied to all the primary inputs of the circuit at the same time. Also, we assume that the signal values

for the internal circuit nodes from the previous test vector have stabilized before the effect of the new test vector reaches them. In other words, a newly applied test vector interacts only with the values resulting from the previous test vector, and not with any other previously applied vector. This has been previously called the *2-vector transition mode of operation* [2]. Hence, a *test* $\bar{v}$ is defined to be a pair of input vectors $\langle v_1, v_2 \rangle$ applied to the circuit in sequence such that the conditions of the 2-vector transition mode of operation are satisfied.

3.2. Delay fault model

To build component delay models which reflect distributed fabrication process effects, we first identify a basis set of fabrication process parameter variations which are *independent* of each other, i.e., which are affected by different process steps. We obtain the probability distribution and range (as determined by some $\pm N$ -sigma variation around the mean) of these fabrication process parameter variations from the statistical characterization data of the fabrication process itself. To a first order of approximation, the process variations are assumed to be global, i.e., the process parameter variations are assumed to be the same throughout the chip. This implies that a *single variable* is sufficient to represent one process parameter variation in all the components of the chip.

We then express each component's delay in terms of these process parameter variations within their range of characterization by using RSM (Response Surface Modeling) techniques. This modeling methodology has been applied to a 2-input gate library. Each function in the delay model for a library gate is of the form $\Delta(\delta_{input}, C_{out}, \mathbf{p})$, where Δ is a polynomial expression in terms of the input transition time (δ_{input}), output load capacitance (C_{out}) and a set of variables ($\mathbf{p} = [w, l, t_{ox}, \dots]$) representing global variations in the process parameters: the variation in channel width (w), the variation in channel length (l), the variation in oxide thickness (t_{ox}), and so on. Since the same set of basis variables is used to characterize each component delay function, the component delays do not vary independently of each other, but are correlated to a large extent. Such a *correlated component delay model* has fewer possible component delay combinations than a model in which each component delay can vary independently within the same individual ranges (as shown in Figure 3 for two component delays $[\Delta_{c0}, \Delta_{c1}]$). The assumption that component delays vary independently of each other within individual $[\min_{\text{component}}, \max_{\text{component}}]$ ranges is commonly used in path sensitization literature in the context of timing verification. We term this model to be an *independently varying component delay model*.

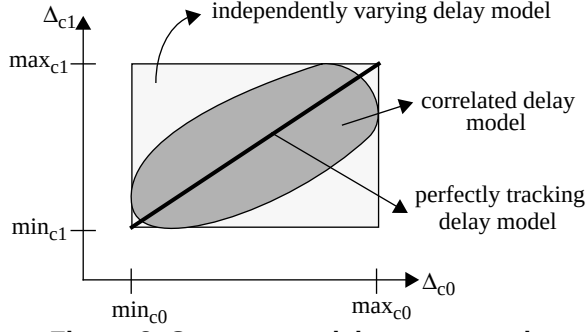


Figure 3. Component delay space under different delay models.

A third kind of a component delay model (also shown in Figure 3), where component delay values track each other completely, is also considered in this paper for the sake of comparison of results. In such a model, for any two components in the circuit, say $c0$ and $c1$, whose delays can vary within the ranges $[\min_{c0}, \max_{c0}]$ and $[\min_{c1}, \max_{c1}]$ respectively, the delay of these components in a particular chip will be $\Delta_{c0} = \min_{c0} + x \cdot (\max_{c0} - \min_{c0})$ and $\Delta_{c1} = \min_{c1} + x \cdot (\max_{c1} - \min_{c1})$, where x is the same for all components, and $0 \leq x \leq 1$. This assumption of perfect linear correlation in all component delay values in the circuit is termed the *perfectly tracking component delay model*. The inspiration for this model comes from the definition of a similar model in [19]. Note however that in that model, all the component delay values in a chip are the same fraction (x) of their respective worst-case (maximum) delay values, and can theoretically be equal to zero (when $x = 0$).

The three component delay models span the component delay space differently (as shown in Figure 3), and therefore yield different kinds of delay fault models and obviously different coverage estimates for a given test set. The correlated component delay model models path delay faults caused by global, distributed fabrication process parameter variations. We term this the *distributed path delay fault model*. The independently varying component delay model and the perfectly tracking component delay model do not model any physical effects of the fabrication process, but are still used in our experiments on benchmark circuits for the sake of comparison.

4. Approach

The strategy for determining delay fault coverage can be divided into two major parts. The first step is to obtain the conditions on the circuit inputs and path delays for which the circuit output exhibits incorrect timing behavior for a given timing constraint T . A path sensitization mechanism based on signal stabilizing times is used to obtain

these delay fault conditions. These delay fault conditions are used to divide the fabrication process parameter variation space into regions where the circuit does not exhibit a delay fault, or has a delay fault which is detectable by the given test set, test , or has delay faults none of which can be detected by test . Once this is achieved, the next step is to compute the integrals $\int f(p) \cdot dp$ inside the appropriate regions, which is performed using a Monte Carlo analysis, to obtain an estimate of the delay fault coverage for the given test set.

4.1. Path sensitization

We use a sensitization scheme, based on the stabilizing times of signal values, to obtain symbolic constraints on path delays and boolean conditions on primary inputs for which the circuit primary outputs stabilize after T , the timing constraint. We calculate the path sensitization conditions leading to a chip failure in one pass for all paths and tests, as opposed to doing so on a path-by-path or test-by-test basis. At each node of the logic-level circuit, we determine the conditions leading to both a late logic-0 stabilization and a late logic-1 stabilization at that node. These conditions at each node are expressed in terms of the possible input vector pairs and symbolic delay constraints on partial paths from the primary inputs leading upto the node. Starting from the primary inputs, a levelized computation of these late signal-stabilizing conditions is performed. The set of such conditions obtained at each primary output is termed as a *delay fault condition expression*, and represents primary input boolean conditions and *and-or expressions* of symbolic path delay constraints for which the stabilizing time of the circuit output is greater than the timing constraint T . This path sensitization mechanism has been explained in greater detail in [14].

4.2. Coverage estimation

After the delay fault condition expressions for the circuit outputs, $DFcond_{ckt}$, have been obtained, the test set, test , for which the delay fault coverage has to be estimated is read in. For each test $\bar{v} \in \text{test}$, the set of symbolic constraints on path delays such that $\bar{v}$ produces a late signal-stabilization at a primary output is represented as $DFcond(\bar{v})$. The constraints on path delays such that some test belonging to test produces a late signal-stabilization at a primary output, $DFcond(\text{test})$, is equal to the set-union $DFcond(\bar{v}1) \cup DFcond(\bar{v}2) \cup \dots$, where $\text{test} = \{\bar{v}1, \bar{v}2, \dots\}$. $DFcond(\text{test})$ is a subset of the path delay conditions contained in $DFcond_{ckt}$, since $DFcond_{ckt}$ represents the circuit output delay fault conditions for *all* tests. $DFcond(\text{test})$ is

not explicitly obtained, but is stored implicitly with $DFcond_{ckt}$.

The delay fault coverage of $\underline{test}$, according to our metric, is the ratio of the integral $\int f(p) \cdot dp$ inside the fabrication process parameter region which satisfies $DFcond(\underline{test})$ to the integral $\int f(p) \cdot dp$ inside the region which satisfies $DFcond_{ckt}$. One can use various numerical techniques to find this ratio from the delay fault condition expressions. We use a Monte Carlo analysis approach to obtain the coverage estimate, as shown in Figure 4. For the correlated

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Given netlist, timing constraint T, find  $DFcond_{ckt}$ .
Read in  $\underline{test}$ .
Find  $DFcond(\underline{test})$ .
loop
{ Generate MCpoint.
  If  $DFcond(\underline{test})$  is satisfied
  { /*  $\underline{test}$  covers delay fault at the MCpoint. */
    covered++.
    total++.
  }
  else if  $DFcond_{ckt}$  is satisfied
  { /*  $\underline{test}$  does not cover the delay fault at the MCpoint. */
    total++.
  }
}
coverage( $\underline{test}$ ) = 100×covered/total.

```

Figure 4. Coverage estimation algorithm.

component delay model (described in Section 3.2), in which component delays are functions of fabrication process parameter variations, the fabrication process parameter combinations are generated in a Monte Carlo fashion. The Monte Carlo points are generated using the joint probability distribution function of the fabrication process parameter variations. Since we choose a basis set of independent process parameter variations in our correlated component delay models, the joint pdf is simply the product of the individual pdfs. The individual component delay values are obtained at a Monte Carlo point by evaluating the component delay functions at the corresponding fabrication process parameter combination. For the independent component delay model, the Monte Carlo points are generated assuming a probability density function for each component within its $[\min_{component}, \max_{component}]$ range. For the perfect tracking component delay model, a Monte Carlo point corresponds to a specific value of the delay fraction x , generated by assuming a probability distribution function for x within its range $[0, 1]$. In this case, the delay value of each component c is evaluated according to the formula $\Delta_c = \min_c + x \cdot (\max_c - \min_c)$.

For the component delay values defined by the Monte Carlo point, we first determine if $DFcond(\underline{test})$ is satisfi-

able. $DFcond(\underline{test})$ is satisfied if $DFcond(\bar{v})$ evaluates to true for some $\bar{v} \in \underline{test}$. This implies that at that Monte Carlo point, $\underline{test}$ will detect the chip failure. However, if $DFcond(\underline{test})$ is not satisfied but $DFcond_{ckt}$ is, $\underline{test}$ fails to cover the chip failure due to a delay fault. This is kept track of at each Monte Carlo point, and after sufficient such points have been generated, the statistical coverage value is evaluated.

5. Experimental results

A prototype version of the statistical path delay fault coverage estimation approach has been implemented. It takes as input a gate level netlist of the circuit, associated component delay models, the timing constraint T, and a test set $\underline{test}$, and estimates the delay fault coverage of the test set under the corresponding component delay model. We have tested this prototype for some ISCAS'89 benchmark circuits. Firstly, a robust path delay fault test generator [7] was used to generate robust tests for these circuits. The robust test generator produces a compact test set where each test can possibly detect more than one path delay fault robustly. The statistical coverages for the robust test sets were obtained under three different kinds of component delay models - the independently varying model, the correlated model, and the perfectly tracking model. The correlated component delay models were built for a certain range of variation of the fabrication process parameters. The minimum and maximum component delay values for the independently varying and perfectly tracking models were obtained by calculating the minimum and maximum delay values of each individual component for the fabrication process parameter variation ranges used in the correlated delay model. Thus, the individual ranges of the component delay variations are the same for all the three models, as shown in Figure 3.

The results for the statistical coverage estimation of the robust test set under the three component delay models are shown in Table 1 for some benchmark circuits. Circuits for which the test generator could find robust tests for all paths are not shown because the statistical delay fault coverage of the robust test set would be 100% regardless of which of the three models were to be used. Also, those circuits for which all the longest paths under our component delay models are robustly testable are not shown, since, for these circuits, the statistical delay fault coverage of the corresponding robust test set will be 100%. The timing constraint T, for most of the benchmark circuits, was set to 80%-90% of the maximum topological (PERT [1]) delay of the circuit i.e., the delay obtained by disregarding path sensitizability. The first 5 columns show the circuit name, the total number of paths in the circuit, the longest topological (PERT) delay with all component delays set to

their individual maximum values, the timing constraint as a percentage of the longest PERT delay, and the number of tests in the robust test set for which the coverage is to be estimated respectively. The sixth column shows the percentage of faulty paths (i.e., those whose delay can be greater than T) which are tested robustly by the robust test set. This would be considered as the coverage of the robust test set under the traditional definition of coverage based on the percentage of paths tested. The next six columns show the statistical delay fault coverage estimates obtained for the three different kinds of component delay models. Furthermore, for each kind of a component delay model, the first column shows the coverage estimate obtained by assuming a truncated Gaussian distribution for the basis parameters of the component delay model (the individual component delay values for the independently varying component delay model, the fabrication process parameter variations for the correlated component delay model, and the delay fraction x for the perfectly tracking component delay model), while the second column shows the coverage estimate obtained by assuming a uniform distribution for the corresponding basis parameters. Finally, the last two columns show the CPU times - the *DFcond* column shows the time taken to generate the delay fault condition expressions for the entire circuit, and the *MCpt* column shows the time taken to process each Monte Carlo point in the coverage estimation procedure.

For many of the circuits, the statistical coverage estimates obtained differ from the robust testability estimates (percentage of faulty paths which are robustly testable) by a large amount. Moreover, there is no obvious correlation in the coverage numbers between the metric based on the percentage of paths tested and our statistical metric, e.g., the circuit s641 has a smaller fraction of its faulty paths robustly testable compared to s298, but the statistical fault coverage for s298 is lower for most of the component delay models. Thus, a coverage metric based solely on the percentage of paths tested is not an accurate measure of

the effectiveness of a test set.

An easily observable fact is that for each circuit, the statistical coverage estimate of the robust test set under the perfectly tracking component delay model is the largest, while the corresponding estimate under the independently varying component delay model is the smallest. This is explained by the following argument. The situation when the robust test set fails to detect a delay fault is when all the robustly testable paths satisfy the timing constraints and some other robustly untestable path/paths do not. This is less likely to happen as the component delays are more correlated, hence the higher statistical coverage estimates for the correlated component delay model and even higher ones for the perfectly tracking component delay model.

The statistical coverage estimates we obtained (shown in the results table) are obviously dependent on the kind of delay faults modeled and the distribution of the fault sizes. Thus, one would expect different results for localized delay defects arising from local fabrication process disturbances, e.g., a local defect on a metal interconnect resulting in a narrow, highly resistive interconnect segment, which retains component functionality but slows it down. Different results can also be expected for distributed path delay faults as a result of different fabrication process parameter variations for each component in a chip, e.g., the channel widths of different devices in the same chip varying by different amounts.

6. Conclusions

We have proposed a very general and realistic statistical delay fault coverage metric based on the percentage of fabricated chips which can be detected as faulty by a given test set. The metric is delay fault model-independent, i.e., it is general enough to be applicable to both gate and path delay fault models. It also takes into account the delay fault size distributions as caused by the fabrication process. As opposed to this, previously defined path delay

Table 1: Delay fault coverage of robust tests.

Circuit	Total paths	PERT (ns)	T	No. robust tests	robust testability	independent		correlated		perfectly tracking		Run time	
						Gaussian	Uniform	Gaussian	Uniform	Gaussian	Uniform	DFcond	MCpt
s1488	1924	24.42	80%	391	85.5 %	100 %	99.89 %	100 %	100 %	100 %	100 %	20 s	0.39 s
s1494	1952	24.56	80%	397	84.7 %	100 %	99.62 %	100 %	100 %	100 %	100 %	20 s	0.38 s
s832	1012	20.11	80%	281	95.8 %	100 %	99.60 %	100 %	100 %	100 %	100 %	4 s	0.13 s
s641	3444	102.83	80%	334	13.4 %	100 %	97.66 %	100 %	100 %	100 %	100 %	3 s	0.24 s
s386	414	17.71	80%	135	98.3 %	100 %	97.81 %	100 %	100 %	100 %	100 %	3 s	0.05 s
s526n	816	13.56	80%	121	25.4 %	100 %	76.59 %	99.78 %	98.61 %	100 %	100 %	1 s	0.05 s
s1423	89452	79.62	90%	7852	9.5 %	1.4 %	2e-52 %	33.75 %	50.54 %	59.05 %	82.70 %	70 s	6.4 s
s298	462	13.56	80%	68	25.4 %	2e-6 %	77.74 %	98.57 %	98.64 %	100 %	100 %	1 s	0.03 s
s444	1070	20.02	80%	112	36.4 %	4e-15 %	34.61 %	3.30 %	21.21 %	36.45 %	70.74 %	3 s	0.05 s
s713	43624	103.29	90%	198	0.1 %	2e-8 %	20.23 %	93.02 %	97.34 %	87.35 %	92.18 %	19 s	0.29 s

fault coverage metrics do not take fault sizes and probability of each path failure into account. Gate delay fault coverage metrics which have attempted to take these into account are limited in scope to single, localized delay defects. Moreover, their applicability to any reasonably sized circuits has not been demonstrated in the literature. We have also presented an approach to implement our metric for estimating the distributed path delay fault coverage of any given test set. This approach uses a path sensitization mechanism based on signal stabilization times, and a Monte Carlo analysis technique for coverage estimation. Results for statistical delay fault coverage estimation of the robust test sets for some ISCAS'89 benchmark circuits have been obtained for the correlated component delay model, which models distributed path delay failures, and two other component delay models. It is seen that the coverage metric based solely on the percentage of paths tested is not an accurate indicator of the effectiveness of a test set. Another significant observation is that the statistical path delay fault coverage of the robust test set is very poor for certain kinds of circuits, the reasons for which have been explained in the previous section. One can conclude from this that while the robust test set shows very good coverages for some circuits, there are other circuits where its delay fault coverage is very poor.

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