# Macromodeling C- and RC-Loaded CMOS Inverters for Timing Analysis

Ayman Kayssi
Department of Electrical and Computer Engineering
American University of Beirut
P.O.Box 11-0236
Beirut, Lebanon

## Abstract

*Timing macromodels for a CMOS inverter loaded by a capacitor or by a series-resistor shunt-capacitor circuit are derived and verified. The macromodel for the capacitive load case is a simple analytical function of a single variable which combines input wave shape, capacitive load, and transistor drive. The model for the RC case is a combination of lookup table and analytical function yielding excellent accuracy to within 5% of detailed circuit simulation.*

## 1. Introduction

The timing analysis of CMOS circuits usually starts with the derivation of a timing model for a CMOS inverter [5][7][13][15]. This approach is due to the simplicity of the CMOS inverter, the insight gained by analyzing an inverter circuit, and the fact that for timing purposes, CMOS gates can be reduced to an equivalent inverter [4]. The majority of CMOS inverter timing models assume a purely capacitive load at the output of the inverter [3][5][13]. While this assumption is valid for inverters driving other CMOS gates with short runs of metal interconnect, it is not valid for inverters driving large loads with long runs of metal interconnect. The load model in this case is a distributed RC line loaded by the input capacitances of the load gates and other lumped capacitances. According to [11] and [12], this load which consists of distributed RC lines and lumped capacitors, can be reduced, using moment matching methods, to a simpler load. The simplified load model consists of a few circuit elements. The number and type of the elements depends on how many moments of the open-circuit input admittance of the RC load are matched. When the first moment is matched, the reduced load model consists of a single capacitor, which, as shown in [12], is the sum of all line and gate input capacitances. When two moments are matched, the reduced load model consists of a series resistor and shunt capacitor. The validity of these approximations has been verified in [11] and [12].

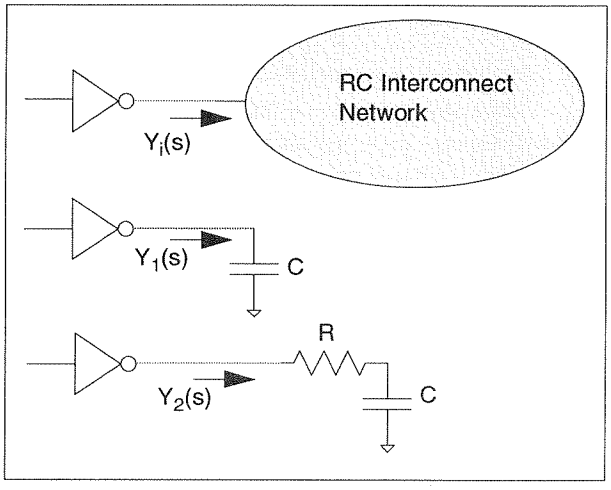


**Figure 1: Input Admittance Models for an RC Interconnect Circuit**

In this paper, timing models for the above-mentionned cases will be derived, namely for a CMOS inverter loaded by a capacitor, or by a resistor-capacitor circuit (see Fig. 1). The macromodels will be derived using dimensional analysis, which greatly reduces the complexity of macromodeling. The paper starts with background material on dimensional analysis in Section 2. In Section 3, a model for a capacitively loaded inverter will be derived. Section 4 presents the model for an RC-loaded inverter. Conclusions are presented in Section 5.

## 2. Dimensional Analysis

Closed-form expressions for the delay of a CMOS inverter cannot be obtained by direct solution of the device



0-8186-7502-0/96 $5.00 

and circuit equations [9]. The delay function can, and usually is, obtained from numerical solutions of the circuit and device equations using circuit simulators such as SPICE [10]. Less frequently, they are determined from direct measurement on actual devices. In either case, "discovering" the functional relation between delay and the factors affecting it can be viewed as experimental model building to which a variety of powerful analysis techniques, such as dimensional analysis [2] and empirical response surface methods [1], can be applied. Dimensional analysis helps identify minimal dimensionless forms of the desired functions; empirical response surface methods are then applied to determine suitable implementations of these functions using curve fitting, lookup tables, or both.

The Pi Theorem of dimensional analysis [2] states that for a given set of $n$ physical magnitudes, measured using $m$ independent fundamental units, the relationship among the magnitudes can be written as *a relationship involving only n-m dimensionless quantities:*

$$f\left(\frac{P_{m+1}}{\prod_{i=1}^{m} P_i^{\alpha_{1i}}}, \frac{P_{m+2}}{\prod_{i=1}^{m} P_i^{\alpha_{2i}}}, \ldots, \frac{P_n}{\prod_{i=1}^{m} P_i^{\alpha_{n-m,i}}}\right) = 0 \qquad (1)$$

Each of the $n$-$m$ arguments of the function $f$ in (1) is called a $\Pi$ number. To calculate the $\Pi$ numbers, we have to compute the $(n\text{-}m)\times m$ matrix $\alpha$ to satisfy the condition that all $\Pi$ numbers are dimensionless. The Pi Theorem, thus, provides a convenient consistency check on presumed functional relations, and may lead to more economical forms of these relations involving fewer arguments. We will make use of the Pi Theorem to simplify the delay equations of C- and RC-loaded CMOS inverters.

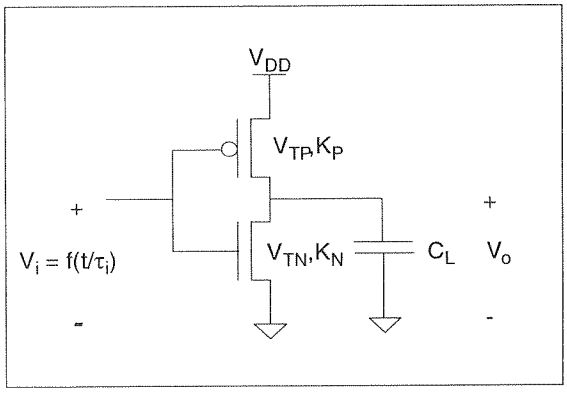


**Figure 2: CMOS Inverter Circuit**

## 3. Capacitively-Loaded Inverters

Consider the CMOS inverter circuit shown in Fig. 2. We are interested in calculating the propagation delay $\Delta$ of a rising signal. Falling signals are treated similarly, since the CMOS inverter has similar rise and fall characteristics. It is appropriate to first define what is meant by gate delay. Fig. 3 shows typical input and output waveforms for a

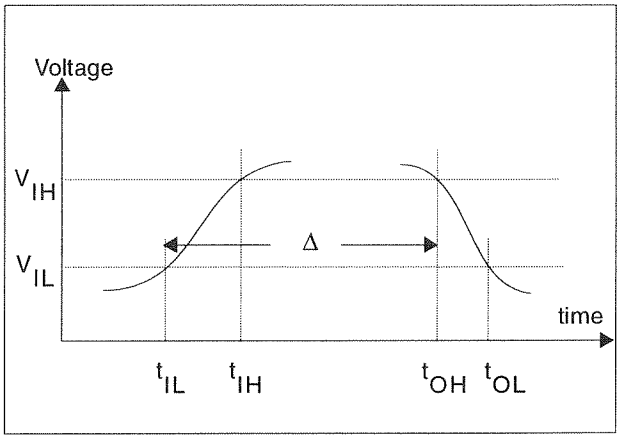


**Figure 3: Definitions of Threshold Voltages and Inverter Delay**

CMOS inverter. The input thresholds at which the differential gain of the inverter is equal to -1 are referred to as $V_{IL}$ and $V_{IH}$ [6]. These two thresholds serve to define the reference times on the input and output voltage waveforms for measuring delay: $t_{IL}$ and $t_{OL}$ are the input time and corresponding output time at which $V_i$ and $V_o$ cross $V_{IL}$; $t_{IH}$ and $t_{OH}$ are the input time and corresponding output time at which $V_i$ and $V_o$ cross $V_{IH}$. Falling gate propagation delay, $\Delta$, is now defined as the time interval between $t_{IL}$ and $t_{OH}$. The choice of the above thresholds for measuring propagation delay, unlike other more commonly used thresholds such as the 50% level of the logic swing insures that $\Delta$ will always be positive.

To model the delay of the CMOS inverter, the following two assumptions are made: First, the model of the MOSFETs corresponds to the LEVEL-1 model in SPICE. Second, the input waveform is assumed to be characterized by a single characteristic time. We will further assume the input waveform to be an exponential function of time, rising from 0 to $V_{DD}$ with a time constant (the characteristic time) equal to $\tau_i$. The results that will be derived are valid for more advanced MOSFET models, including short-channel (alpha-power law) models, and for any input wave shape, as long as it is characterized, similar to an exponential function, by a single characteristic time [9].

The parameters affecting the delay of the CMOS inverter are the capacitance $C_L$, the supply voltage $V_{DD}$, the transconductances of the N and P-channel MOSFETs ($K_N$ and $K_P$, respectively), the N- and P-channel threshold voltages, $V_{TN}$ and $V_{TP}$, respectively, the thresholds at which the delay is being measured, and the time constant of the input waveform $\tau_i$. The delay function can therefore be written as:

$$\Delta = f(C_L, V_{DD}, K_N, K_P, V_{TN}, V_{TP}, V_{IL}, V_{IH}, \tau_i) \quad (2)$$

Applying the Pi Theorem to the delay function with $V_{DD}$, $K_N$, and $\tau_i$ as primary quantities yields the following reduced function:

$$\frac{\Delta}{\tau_i} = f\left(\frac{C_L}{K_N V_{DD} \tau_i}, \frac{K_P}{K_N}, \frac{V_{TN}}{V_{DD}}, \frac{V_{TP}}{V_{DD}}, \frac{V_{IL}}{V_{DD}}, \frac{V_{IH}}{V_{DD}}\right) \quad (3)$$

For a given process and supply voltage, $V_{TN}/V_{DD}$ and $V_{TP}/V_{DD}$ are constants. Moreover, since CMOS inverters are designed so that they have symmetrical rise and fall characteristics, $K_P/K_N$, $V_{IL}/V_{DD}$, and $V_{IH}/V_{DD}$ are constants. Therefore, the delay function can be simplified to a function of a *single* independent variable $C_L/(K_N V_{DD} \tau_i)$ that combines the effects of capacitive loading, input time constant, and transistor drive capability:

$$\frac{\Delta}{\tau_i} = f\left(\frac{C_L}{K_N V_{DD} \tau_i}\right) \quad (4)$$

Dimensional analysis has thus simplified the function to a single-argument one. The exact form of the function cannot be determined by dimensional analysis alone.

Experiments to determine the function $f$ were conducted by running circuit simulations on inverter circuits with varying capacitive load, input time constant, and N-channel MOSFET transconductance. The values of $C_L$ were randomly chosen between 0.01 and 1 pF, the values of $\tau_i$ were randomly chosen between 0.01 and 1ns, and the values of the width of the NMOS transistor $W_N$ were randomly chosen between 10 and 150 μm. The channel lengths of the MOSFETs were fixed at $L_N = L_P = 2$ μm. The values of the remaining parameters which do not change in the simulations were as follows:

$V_{DD} = 5$ V
$k'_N = 2k'_P = 30$ μA/V$^2$
$V_{TN} = -V_{TP} = 0.7$ V
$\lambda_N = \lambda_P = 0.05$ V$^{-1}$
$V_{IL} = 1.963$ V
$V_{IH} = 3.037$ V

The width of the PMOS transistor was chosen to be twice that of the NMOS transistor, in order to obtain symmetrical rise and fall characteristics. The values of $V_{IL}$ and $V_{IH}$ were calculated from a DC analysis of such a symmetrical CMOS inverter.

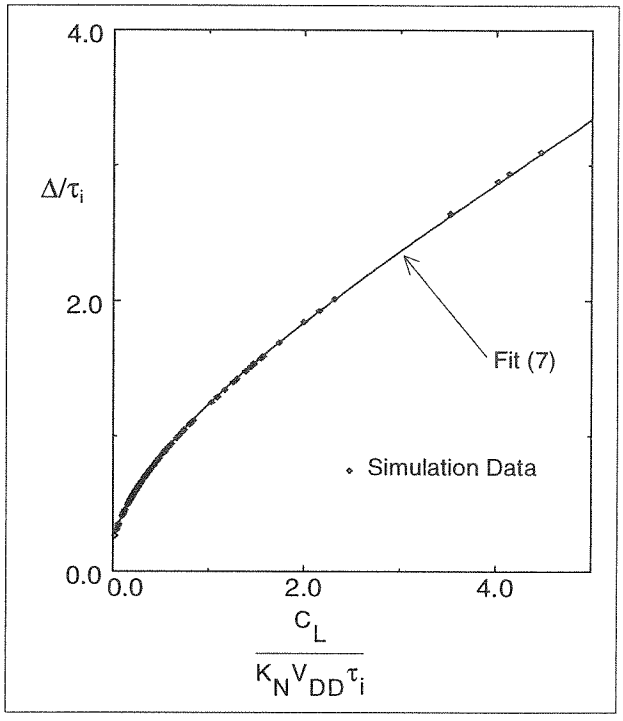


**Figure 4: Delay of a Capacitively-Loaded CMOS Inverter**

The data obtained from the simulation was plotted as shown in Fig. 4. The plot clearly shows that there is no scattering in the data, even though the parameters $C_L$, $\tau_i$, and $W_N$ were chosen randomly from the ranges listed above. After experminentation with different fitting functions in Mathematica [14], the following functions provided excellent curve fits:

$$f_1(x) = \frac{a_0 + a_1 x + a_2 x^2}{b_0 + b_1 x + b_2 x^2} \quad (5)$$

and

$$f_2(x) = a_0 + a_1 x + a_2 x^2 + a_3 \sqrt{x} \quad (6)$$

For the particular technology parameters used in the simulation, the following fitting functions were obtained:

$$f_1(x) = \frac{1.72709x^2 + 5.75587x + 0.744851}{0.00148851x^2 + 3.77134x + 2.85585} \quad (7)$$

and

$$f_2(x) = 0.150868 + 0.296945x + 0.00147497x^2 + 0.773175\sqrt{x} \quad (8)$$

The quality of the fit in both cases is excellent and both functions provide exceptionally accurate fits to the delay of a capacitively-loaded CMOS inverter. For 1500 test circuits, the predictions of (7) and (8) were compared with circuit simulation data. The relative errors (defined as $(\Delta_{\text{circuit simulation}} - \Delta_{\text{equation}})/\Delta_{\text{circuit simulation}}$) in the case of (7) were normally distributed with a mean of 0.066735 and a standard deviation of 1.5968. In the case of (8) the mean was 0.17343 and the standard deviation 1.0516. In both cases the errors are within 5%. We chose to use (7) since it involves simple arithmetic operations, while (8) includes a square root term, which is computationally an expensive operation.

## 4. RC-Loaded Inverters

The inclusion of a series resistor in the model of the load that the CMOS inverter is driving introduces an extra argument to the delay function (2). By applying the Pi Theorem and going through the same steps as we did for the case of the simple capacitive load, the following delay function is obtained:

$$\frac{\Delta}{\tau_i} = f\left(\frac{C_L}{K_N V_{DD} \tau_i}, RK_N V_{DD}\right) \quad (9)$$

For convenience, we will write this equation as $y=f(x,z)$ where $y \equiv \Delta/\tau_i$, $x \equiv C_L/(K_N V_{DD} \tau_i)$, and $z \equiv RK_N V_{DD}$.

By simulating the RC-loaded CMOS inverter circuit at different values of $z$, it was observed that the dependence of $y$ on $x$ can always be fitted using a function of the form (5), irrespective of the value of $z$. Therefore, by making the fitting coefficients in (5) functions of $z$, we can model the effect of the variable $z$, and therefore the resistance $R$. The same functional form for the fitting function is thus used:

$$f_1(x,z) = \frac{a_0(z) + a_1(z)x + a_2(z)x^2}{b_0(z) + b_1(z)x + b_2(z)x^2} \quad (10)$$

Since the fitting coefficients are now functions of $z$, it is possible to, in turn, fit the coefficients to analytical functions of $z$. However, it was found more appropriate to use a piecewise linear table approximation whereby, as shown in Table 1, the dependence of $y$ on $x$ is shown analytically at different values of $z$, referred to as the table breakpoints. For values of $z$ not equal to the breakpoints, linear interpolation is used to calculate $y$. The breakpoints were calculated using the procedure described in [8]. This procedure ensures that the maximum error due to the linear interpolation is always less than a certain preset error limit. The breakpoints shown in Table 1correspond to a maximum linear interpolation error of 5%. For a maximum interpolation error of 10%, the size of the table is reduced, and only the following breakpoints are included: 0.000, 0.412, 0.506, 0.678, 1.040, 2.000.

| z | Fitting Function $y=f(x)$ |
|---|---|
| 0.000 | $(445.34x^2 + 1386.52x + 181.634) / (x^2 + 946.58x + 682.558)$ |
| 0.412 | $(8.71469x^2 + 48.4878x + 5.32391) / (x^2 + 44.6299x + 22.266)$ |
| 0.506 | $(3.04974x^2 + 10.4998x + 0.855126) / (x^2 + 11.8931x + 3.94394)$ |
| 0.594 | $(1.91101x^2 + 5.4393x + 0.510691) / (x^2 + 6.58459x + 2.16766)$ |
| 0.678 | $(1.43542x^2 + 2.90722x + 0.241223) / (x^2 + 3.96105x + 1.05665)$ |
| 0.852 | $(1.00928x^2 + 1.04772x + 0.0623994) / (x^2 + 1.80399x + 0.296028)$ |
| 1.040 | $(0.803398x^2 + 0.656349x + 0.0450723) / (x^2 + 1.2446x + 0.195619)$ |
| 1.490 | $(0.58082x^2 + 1.82153x + 0.129707) / (x^2 + 3.4201x + 0.581748)$ |
| 2.000 | $(0.46531x^2 + 2.03778x + 0.106296) / (x^2 + 4.55336x + 0.500317)$ |

**Table 1: Interpolation Table for the Delay of an RC-Loaded CMOS Inverter**

The quality of the delay macromodel for RC-loaded CMOS inverters is illustrated by the error scatter plot in Fig. 5. For 1500 randomly-generated test circuits, the relative error is always within 5%. The errors in this case are not normally distributed, due to the piecewise linear function approximation.

## 5. Conclusions

We have derived delay macromodels for CMOS inverters driving either a capacitor or a series-resistor, shunt-capacitor circuit. We showed the delay of the capacitively-loaded CMOS inverter to be a function of a single variable

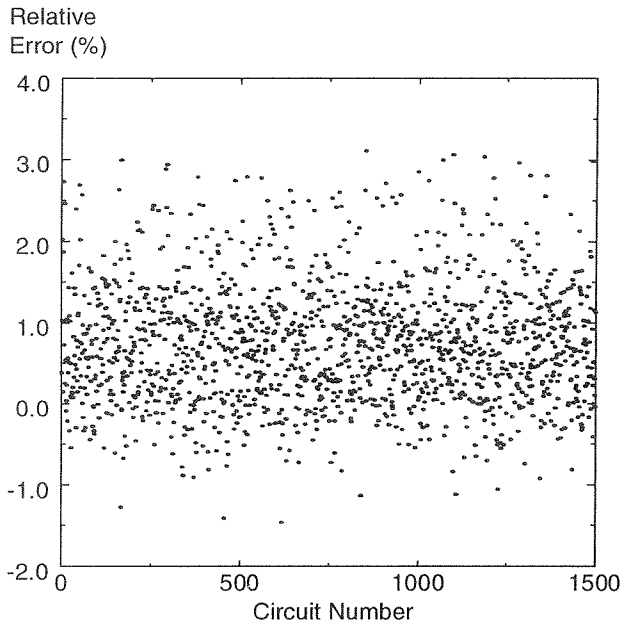


**Figure 5: Scatter Plot for Relative Errors in Delay Model of the RC-Loaded CMOS Inverter.**

which combines capacitive load, inverter drive capability, and input wave shape. A rational function provided an excellent fit to simulation data with a maximum relative error of 5%. For the case of RC-loaded CMOS inverters, the delay function depends on an extra variable, which varies with the resistance value. A combination of table lookup and analytical function fit provides an excellent fit in this case. The errors in the case of the RC load are also within 5% of circuit simulation.

## References


[1] G. E. Box and N. R. Draper, *Empirical Model-Building and Response Surfaces*, John Wiley & Sons, 1987.

[2] E. Buckingham, "Model Experiments and the Forms of Empirical Equations," *Transactions of the ASME*, vol. 37, pp. 263–296, 1915.

[3] J. R. Burns, "Switching Response of Complementary-Symmetry MOS Transistor Logic Circuits," *RCA Review*, vol. 25, pp. 627–661, December 1964.

[4] H. Y. Chen and S. Dutta, "A Timing Model for Static CMOS Gates," in *Digest of Technical Papers of the IEEE International Conference on Computer-Aided Design*, pp. 72–75, 1989.

[5] N. Hedenstierna and K. O. Jeppson, "CMOS Circuit Speed and Buffer Optimization," *IEEE Transactions on Computer-Aided Design*, pp. 270–281, March 1987

[6] D. A. Hodges and H. J. Jackson, *Analysis and Design of Digital Integrated Circuits*, McGraw-Hill, 1983.

[7] B. Hoppe, G. Neuendorf, D. Schmitt-Landsiedel, and W. Specks, "Optimization of High-Speed CMOS Logic Circuits with Analytical Models for Signal Delay, Chip Area, and Dynamic Power Dissipation," *IEEE Transactions on Computer-Aided Design*, pp. 236–247, 1990.

[8] A. I. Kayssi, *A Methodology for the Construction of Accurate Timing Macromodels for Digital Circuits*, PhD Thesis, University of Michigan, May 1993.

[9] A. I. Kayssi, K. A. Sakallah, and T. M. Burks, "Analytical Transient Response of CMOS Inverters," *IEEE Transactions on Circuits and Systems*, January 1992.

[10] L. W. Nagel, "SPICE2, A Computer Program to Simulate Semiconductor Circuits," Technical Report ERL-M520, University of California, Berkeley, 1975.

[11] P. R. O'Brien, J. L. Wyatt, T. L. Savarino, and J. M. Pierce, "Fast On-Chip Delay Estimation for Cell-Based Emitter Coupled Logic," in *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 1357–1360, 1988.

[12] P. R. O'Brien and T. L. Savarino, "Modeling the Driving-Point Characteristic of Resistive Interconnect for Accurate Delay Estimation," in *Digest of Technical Papers of the IEEE International Conference on Computer-Aided Design*, pp. 512–515, 1989.

[13] T. Sakurai and A. R. Newton, "Alpha-Power Law MOSFET Model and its Applications to CMOS Inverter Delay and Other Formulas," *IEEE Journal of Solid-State Circuits*, pp. 584–594, April 1990.

[14] S. Wolfram, *Mathematica*, Addison-Wesley, 1988.

[15] H. G. Yang and D. M. Holburn, "Switch-Level Timing Verification for CMOS Circuits: A Semianalytic Approach," *IEE Proceedings*, pp. 405–412, December 1990.