A 3V-50MHz Analog CMOS Current-Mode High Frequency Filter with A Negative Resistance Load

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Abstract

A low voltage Analog CMOS current-mode continuous-time high frequency filter with a negative resistance load (NRL) is proposed. To design a current integrator, we use a modified simple current mirror with a NRL to increase the output resistance. The current integrator is designed to have the frequency behavior enhancement and operate in low voltage by employing a simple mirror structure and diode connected input transistor. The third order Butterworth low pass filter using a current integrator is synthesized and simulated with a 1.5μm n-well process. Simulation result shows cutoff frequency of 50 MHz and power consumption of 2.4mW/pole with a 3V power supply.

1. Introduction

Several analog CMOS continuous-time filters for high frequency applications have been reported in the literature[1]-[11]. Most of these filters were designed to process voltage signals. It results in high voltage power supply and large power dissipation. To overcome these drawbacks of the voltage-mode filters, the current-mode filter circuits, which process current signals, have been developed[3,5,11]. Some of these current-mode filters have employed cascode current mirrors to implement a current integrator. However, four stacked transistors in the current integrator require high power supply voltage. And many internal nodes prevent the current integrator from operating at very high frequency range.

In order to reduce a magnitude of power supply voltage, a NRL current integrator is proposed to design a current-mode low pass filter for high frequency application. The NRL current integrator, which is the counter part of the voltage-mode NRL integrator[4,11], consists of basic current mirrors and negative resistance loads to generate high impedance nodes and minimum number of internal nodes.

2. Current integrator with a NRL

A circuit diagram of the differential input/differential output NRL current-mode integrator with basic current mirrors is shown in Fig. 1. The integrator consists of two modified basic current mirror circuits, mirror1(M1, M2, M3, M4) and mirror2(M11, M12, M13, M14), and two NRL circuits(M5, M6, M7, M8 and M15, M16, M17, M18).

The current gain transfer function of the integrator in Eqn (1) can be obtained by analyzing the small signal model for the half circuit of the NRL current integrator, as illustrated in Fig. 2.

\[
\frac{I_{out}}{I_{in}} = \frac{g_{m, out} - g_{o, out}}{g_{m, in} + g_{o, in}} \cdot \frac{(1 - s) c_D + 2c_B}{(1 + c_E + c_D + 4c_B)} = A \frac{Z_1}{1 + \frac{s}{p_1}}
\]

Where

- \( c_D = c_{gD} + c_{gA} + c_{bD} + c_{bA} + c_{bD} + c_{bA} + c_{bD} + c_{bA} + c_{bD} + c_{bA} + c_{bD} + c_{bA} \)
- \( c_B = g_{m, D} + g_{m, A} + g_{m, D} + g_{m, A} + g_{m, D} + g_{m, A} + g_{m, D} + g_{m, A} \)
- \( g_{m, in} = g_{m, out} \approx g_{m, in} \approx g_{m, out} \approx g_{m, in} \approx g_{m, out} \approx g_{m, in} \approx g_{m, out} \approx g_{m, out} \approx g_{m, in} \approx g_{m, out} \)

A is the dc current gain, \( p_1 \) is the dominant pole, and \( Z_1 \) is the zero.

Two gate to drain connected transistors(M1, M3 or M11, M13) in each mirror, are employed to increase an transconductance of each mirror that is each current amplifier, consequently, an bandwidth of the integrator. As the zero point \( Z_1 \) is proportional to the transconductance \( g_{m, out} \) of each mirror, the bandwidth can be enhanced by \( 1 + g_{m, out} / g_{o, out} \)BW. Where \( BW \) is the bandwidth of the integrator using the basic current mirror that has only one gate to drain connected transistor. The designed circuit takes advantage of the bandwidth enhancement at the expense of the relatively large DC voltage drop. \( 2V_{DSAT} + 2V_{th} \) across M1 and M3 than the that of the basic
current mirror, \(2V_{\text{dss}} + V_{\text{th}}\). Another advantage of utilizing two gate to drain connected transistors is that it does not require the extra bias circuit.

3. Negative resistance load

Another problem of employing the basic current mirror in the current integrator is that the dc current gain of the integrator is unable to exceed 40 dB due to the dc gain of \((g_m / 2g_{ds})[5]\). The proposed current NRL circuit is capable of enhancing the DC-gain of the integrator over 60 dB. The MOSFETs (M5, M6, M7 and M8) construct a current NRL circuit. Because the current integrator operates in the differential mode, the input node voltage possesses the same magnitude of the output node voltage with the opposite sign. Applying KCL to the input and output nodes of the mirror1 in the condition of dc characters, Eqn. (2) and Eqn. (3) are obtained by:

\[
\begin{align*}
I_{\text{in}+} + I_{\text{out}} &= (g_{m5} + g_{m6} + g_{m7} - g_{m5} + g_{m6} + g_{m7} + g_{ds})V \\
&= (g_{m6} + g_{sh} + g_{ds})V \\
I_{\text{out}} &= (g_{m5} + g_{m6} + g_{m7} - g_{m5} + g_{m6} + g_{m7} + g_{ds} + g_{ds})V \\
&= (g_{m7} + g_{ds} + g_{ds})V
\end{align*}
\]  

In Eqn. (2) and Eqn. (3), two terms, \(g_{m5} - g_{m6}\) and \(g_{m7} - g_{m6}\) can be rewritten by:

\[
g_{m5} - g_{m6} = g_{m7} - g_{m6} = \mu_p C_{ox} S_5 (V_C - V_{DD})
\]

where \(S_5\) is the device aspect ratio of the MOSFET M5. The NRL circuit can be achieved by making \(V_C\) smaller than \(V_{DD}\). The proper tuning of \(V_C\) makes it possible to satisfy Eqn. (5).

\[
\mu_p C_{ox} S_5 (V_{DD} - V_C) = g_{ds1} + g_{ds3} + g_{ds5} + g_{ds6} \\
= g_{ds2} + g_{ds4} + g_{ds7} + g_{ds}
\]

In other words, \(g_{ds,\text{in}}\) and \(g_{ds,\text{out}}\) can be made to be close zero. The resultant dc current gain of the NRL integrator is \((g_{m2} + g_{m3}) / (g_{ds,\text{in}} + g_{ds,\text{out}})\) and can be ideally reached to the infinity. In order to generate the large dc gain, it is required to generate the smallest value of \((g_{ds,\text{in}} + g_{ds,\text{out}})\) as possible. To make it happen, two parameters, \(S_5\) and \(V_C\) in Eqn. (5) need to be finely controlled.

4. Active filter synthesis

A third order Butterworth low pass filter with the bandwidth of 50MHz has been realized by employing the designed NRL current integrator. The doubly terminated third order passive low pass filter, as shown in Fig. 3, is utilized to synthesize the associated active filter[12], as illustrated in Fig. 4. The integrators(INT1, INT2, INT3) are the identical NRL current integrator designed in Fig. 1. In the synthesized active filter circuit, it is noted that the output of the integrators is connected to the input of the adjacent integrator. The connection is achieved by adding an extra current mirror to the designed NRL integrator circuit.

The dominant pole, \(P_1\) and the gain-bandwidth product, \(f_A\) of the NRL current integrator are controlled by the input integration capacitor, \(C_1\).

\[
C_1 = \frac{g_{mi,\text{out}} X_{\text{normalized}}}{2\pi f_0} - C_{\text{parasitic}}
\]

where \(C_{\text{parasitic}}\) is a parasitic capacitance on the input node of the integrator and \(C_{\text{parasitic}} + 4C_{B}\). \(g_{mi,\text{out}}\) is a transconductance of the modified basic current mirror, \(f_0\) is the mapping frequency, and \(X_{\text{normalized}}\) is a normalized each element value of passive network.

The frequency response of the NRL current integrator are plotted in Fig. 5 as a function of \(V_C(2.76V, 2.77V, 2.78V, 2.79V)\). The simulation results show that the condition of \(V_C = 2.76\) satisfies Eqn. (5) to generate the highest dc gain of the designed NRL current integrator. The magnitude bode plots of the third order active filter as a function of \(V_C\) are shown in Fig. 6. The zoomed plot in the box illustrates that the variation of \(V_C\) rarely affects the filter response. The simulation results of the active filter are summarized in Table 1. Also, the electrical performances of the designed filter are compared with those of the other voltage-mode and current-mode filters in Table 2. The layouts of the current integrator and filter with NRL circuit are illustrated in Fig. 7 and Fig. 8, respectively.

5. Conclusion

A current-mode NRL integrator is designed to implement the third order Butterworth low pass filter with the bandwidth of 50MHz. Since the designed integrator consists of the modified basic current mirrors and NRL circuits, it requires low voltage(3V) and low power dissipation(2.4mW/pole). The inherent circuit structure, which minimizes the internal circuit nodes and enhances the gain-bandwidth, makes the filter operate at the high frequency. Because of no bias circuits and basic current mirror, the chip area in the layout of the third order low pass filter only occupies 1mm².
REFERENCES


Table 1. Simulation results of the synthesized filter

<table>
<thead>
<tr>
<th>Process</th>
<th>CMOS n-well 1.5μm</th>
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<tr>
<td>Power Supply</td>
<td>3 V</td>
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<tr>
<td>3dB cutoff frequency</td>
<td>50MHz</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>2.4mW/pole</td>
</tr>
<tr>
<td>Active Transistor Gate Size</td>
<td>560 μm²/pole</td>
</tr>
</tbody>
</table>

Table 2. Comparison of the filters for high frequency

<table>
<thead>
<tr>
<th></th>
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</tr>
</thead>
<tbody>
<tr>
<td>Power Supply</td>
<td>5 V</td>
<td>5 V</td>
<td>3 V</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>2.7 mW/pole</td>
<td>11mW/pole</td>
<td>2.4 mW/pole</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>50 MHz</td>
<td>63MHz</td>
<td>50MHz</td>
</tr>
<tr>
<td>the position of parasitic pole or zero</td>
<td>100GHz</td>
<td>10GHz</td>
<td>1GHz</td>
</tr>
<tr>
<td>Process</td>
<td>2 μm CMOS</td>
<td>3μm CMOS</td>
<td>1.5μm n-well CMOS</td>
</tr>
<tr>
<td>Building Block</td>
<td>gm-C</td>
<td>gm-C</td>
<td>Current Integrator</td>
</tr>
</tbody>
</table>

Fig. 1. The circuit schematic of the designed current integrator with NRL

Fig.2. The small signal equivalent circuit of the half circuit of the current integrator

Fig 3. A circuit diagram of third order passive Butterworth low pass filter
Fig. 4. A circuit diagram of the current-mode NRL active filter.

Fig. 5. The simulation results of the designed current integrator ($V_C$: external tuning voltage).

Fig. 6. The frequency response of the third order Butterworth low pass filter with bandwidth of 50Mhz.

Fig. 7. Layout of the current-mode NRL integrator.

Fig. 8. Layout of the current-mode NRL active filter.