A High Speed, Real-to-Quadrature Converter with Filtering and Decimation

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Abstract

The design of a high speed, real-to-quadrature converter chip set with filtering, decimation, built-in self-test (BIST), and IEEE 1149.1 based boundary scan will be presented. The 15,000 gate application specific integrated circuit (ASIC) implemented in 1.5 μm CMOS gate array technology has 3 half-band filters with 3, 7, and 11 taps which can be cascaded in a number of combinations. The intended ASIC application is the processing of narrowband radio signals at IF frequencies. The paper addresses the ASIC’s functionality, VLSI implementation and test methodology, and provides both simulation and test data.

1. Introduction

VLSI implementation of digital signal processing (DSP) algorithms, for real time applications such as digital radio receivers has become possible through the exploitation of novel architectures and advanced CMOS technology. The signal processing requirements associated with signal filtering, demodulation, decoding, and protocol handlings are normally executed by means of generic or dedicated processors operating at baseband. In the last few years, with improvements in both ADC and low power CMOS technology, it has become possible to extend the digital processing to IF frequencies. In such designs, the incoming IF signal is sampled at twice or four times the signal frequency and the narrowband sampled signal is filtered and downconverted to baseband where the decimated signal is demodulated and processed [1]. To facilitate the filtering and downconversion of the sampled IF signal, it is frequently converted into its analytical representation by means of a real-to-quadrature (RQ) converter which is followed by a few stages of filtering and decimation. The filtering and decimation are carried out independently on the inphase and quadrature channels.

The real-to-quadrature conversion is implemented by sampling the signal at four times its center frequency and downconverting to complex baseband. In the process the sampling rate of the signal is reduced by a factor of four.

This technique [2], [3] has the advantage of requiring multiplication of the incoming signal by only ± 1.

The programmable ASIC incorporates the real-to-quadrature converter but only one set of filters. Thus to implement a full real-to-quadrature converter, two devices are utilised with one device filtering and decimating the inphase signal and the other operating on the quadrature signal. The device can be programmed to operate in different modes and can accept either a real input or a complex input. In the latter case, because the signal has already been converted to its analytical representation, the on-board real-to-quadrature conversion circuit is bypassed and the signal is simply filtered and decimated. Figure 1 depicts a typical configuration in which the real-to-quadrature ASIC accepts high speed data samples from an ADC, converts the signal to its analytical representation, downconverts it to baseband, and filters and decimates the signal. To obtain fine frequency tuning, the signal is routed to a complex multiplier for mixing with a reference signal from a numerical control oscillator (NCO). The 15,000 gate ASIC is implemented in a 1.5 μm, LSI Logic LMA9K gate array.

2. ASIC architecture

The real-to-quadrature chip has a data path architecture with the signal filtering and routing taking place at clock rates that are equal to 1, 1/2, 1/4, 1/8 or 1/16 of the master clock frequency to which they are synchronized. The design incorporates three half-band filters with integer coefficients which permit the implementation of all multiplications by means of hardwired shifts and addictions. Furthermore, the half-band filters are symmetric and nearly half of their coefficients are zero, making them particularly suitable for implementation in multirate filters [4], [5].

In each of the three filters and the RQ module, the arithmetic operations are combined in one arithmetic module which facilitates their optimization. The output of each block is accompanied by a strobe pulse that is used to clock the data into the next block.

The real-to-quadrature ASIC in figure 2 has two 8 bit inputs, I and Q, and one 16 bit input, D. Both I and Q inputs are used when complex signals are input, i.e.,
when the real to quadrature conversion is performed externally. Otherwise, the I port is used for the real 8 bit input and the Q input is grounded. For either case of real or complex signal inputs, either the I or Q portion of the signal is made available at the output port C.

As the multiplexers denoted in Figure 2 are independently controlled, the chip can be configured to support two independent data paths from the input to the output. Thus it is feasible to perform real-to-quadrature conversion on the real input with either the I or Q provided at port C and, concurrently, filter and decimate the signal input at port D. In the latter case, the resulting filtered and decimated signal would be routed to port M.

The RQ block, shown in Figure 3, contains the bulk of the ASIC's high speed circuitry. The I and Q inputs are fed into a series of registers and relocked at half the input data rate by a multiplexed register. This multiplexed register determines whether this ASIC acts as the inphase or quadrature part of the system. In order to meet the high throughput requirement, 4 pipeline registers were inserted in the RQ block. The RQ adder was optimized for performance for a maximum throughput rate of 114 Msamples/s. The 10 bit wide, decimated by 2 output of RQ can be connected to all three filters and the C output.

H1 is a high pass, half-band FIR filter of order 3 whose block diagram is depicted in figure 4. The coefficients for this filter are: \(h(±1) = -1\) and \(h(0) = 2\). This filter suppresses the signal image and reduces the noise and interference signals prior to signal decimation. It's input can come from the output of RQ or from the 16 bit wide input D and is rounded off to 10 bits at the input to H1. The output is 13 bits wide and can be connected to the H2 and H3 filters and the C and M outputs. The decimation by two is done at the input to H1, thus enabling the adder to work at one half of the input data rate. The H1 filter has 4 pipeline registers to increase its data throughput rate. Furthermore, the H1 adder was optimized for performance for a maximum throughput rate of 89.5 Msamples/s.

Figure 5 depicts H2, a low pass, half-band FIR filter of order 7, whose input can come from RQ, H1, or the input D. The input of H2 is rounded off to 13 bits. The coefficients for this filter are: \(h(±3) = -1, h(±2) = 0, h(±1) = 8, \) and \(h(0) = 14\). The output is 16 bits wide and can be connected to H3, the output C, and the output M. H2 has one level of pipelining to increase its throughput. The H2 adder was optimized for performance for a maximum throughput rate of 53.7 Msamples/s.

H3, shown in figure 6, is a low pass, half-band FIR filter of order 11 whose input comes from RQ, H1, H2, or the D input port. The coefficients for this filter are: \(h(±5) = 1, h(±4) = 0, h(±3) = -5, h(±2) = 0, h(±1) = 24, \) and \(h(0) = 40\). The output is 16 bits wide and can be connected to the C and M outputs. H3 has one level of pipelining and the H3 adder was optimized for performance for a maximum throughput rate of 40.0 Msamples/s.

The output C is 12 bits wide and can be driven by the outputs of RQ, H1, H2, or H3. The output M is 16 bits wide and can be driven by the outputs of H1, H2, H3, or by the input port D. Both outputs can be tri-stated independently of each other.

The configuration of the ASIC is controlled by two 8 bit registers in the CONTROL block. The CONTROL block is responsible for the routing of data to all three filters and the two output multiplexers as well as for determining whether the ASIC filters the quadrature or the inphase signal.

3. BIST Implementation

The ASIC design includes built-in self-test circuitry (BIST) and the IEEE 1149.1 boundary scan standard [6], [7]. The purpose of the BIST circuit was to test the core of the ASIC, excluding the IEEE boundary scan, and to enable the easy determination of the maximum internal speed of the ASIC without using an expensive, high speed IC tester. There are three, linear feedback shift register (LFSR) based, pseudo random number generators located at the inputs of the I, Q and D data ports. The multiple input signature register (MISR) based compactor is fed from the C and the M ports. A sequencer is used to test 8 different data path combinations, each having it's own signature. This enables all data paths between the blocks to be tested. The signatures were chosen to maximize the toggle coverage for each configuration and, as a result, each of the 8 sequences are of different length. Toggle coverage for the ASIC core is 100% and fault coverage is 87.8%.

4. Optimization and Results

The RQ block and the three filters have been optimized for performance with the Mentor Graphic's Autologic tool. It is the arithmetic modules of the filters and the RQ module that have been optimized. Table 1 summarizes the optimization results and provides the maximum frequency under worst case commercial conditions for each block.

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<td>Functional Block</td>
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The optimized frequencies chosen for each filter were selected taking into consideration the available number of gates and the location of each block in the filter chain.

Simulation results have shown that the ASIC depicted in Figure 7 has a maximum input data rate of 58 Mhz under worst case commercial conditions. Test results
showed the devices to be operating at a maximum input data rate of 35.7 MHz for the functional set of vectors and 63.5 MHz in self test mode. These test results were obtained with an IMS XL-100 IC tester. The discrepancy between the simulation and actual test results can be attributed to the increased capacitive loading present in the test fixtures. The output load in the test setup was over 100 pF for each output pin as compared to 35 pF employed in the simulations.

5. Summary

A 15,000 gate, pipelined, high speed real-to-quadrature converter with filtering and decimation has been designed. Judicious partitioning of the circuit and the incorporation of programmability and flexible data routing permits the two-chip-set-implementation to be used in a wide range of applications and configurations. Test results showed that, in self-test mode, the ASIC's core circuitry is capable of operating at 63.5 MHz.

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References
