Input Pattern Classification for Transistor Level Testing of Bridging Faults in BiCMOS Circuits

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Abstract

Combining the advantages of Bipolar and CMOS, BiCMOS is emerging as a major technology for high speed, high performance, digital and mixed signal applications. Recent investigations have revealed that bridging faults can be a major failure mode in ICs. This paper presents effects of bridging faults affecting p- or n-parts and input bridging faults of logical nodes affecting p- and n-parts. It is shown that bridging faults can be detected by \( I_{DDQ} \) monitoring in BiCMOS devices. An input pattern classification scheme is presented for bridging faults. These classes of input patterns are then used to obtain test sets for bridging fault detection.

1 Introduction

Combining the advantages of CMOS and bipolar, BiCMOS is emerging as a major technology for many high performance digital and mixed signal applications. The main advantages of CMOS technology over bipolar are lower power dissipation and higher packing density. Bipolar technology offers better output current drive, switching speed, I/O speed and analog capability. Combining the advantages of bipolar and CMOS, BiCMOS offers the following advantages [1]: improved speed over CMOS, lower power dissipation compared to bipolar, flexibility in I/O (TTL, ECL, CMOS compatibility), high performance analog capability and latch up immunity. Compared to the CMOS counterparts, BiCMOS circuits can be faster by a factor of up to two for the same level of technology. Access times of less than 10ns have been reported for 0.8 \( \mu m \) BiCMOS ECL input/output 256K and 1M-bit SRAMs [2]. 100K gate arrays operating at 100MHz clock rates have also been reported [2]. BiCMOS is even being considered for high performance microprocessors and dynamic RAMs, and it is felt that it will be one of the main technologies to drive almost all functions in the decade ahead [3].

Most of the defects and failures in present day integrated circuits can be abstracted to shorts and opens in the interconnects and degradation of devices [4]. Transistor level shorts and opens model many of the physical failures and defects in ICs [5]. A study by Gallay [6] on 4-bit MOS microprocessor chips revealed that many of the faults were shorts and opens at the transistor level. Analysis of faults in elementary static storage elements suggest that transistor level testing provides a higher coverage of faults compared to that at the gate level [7]. Thus, it is necessary to study the effects of failures at the transistor level and develop accurate fault models at this level [5]. The major fault models at transistor level are stuck-at faults, and shorts and opens of transistors and interconnects [8]. It has been shown [9]-[14] that the stuck-at model does not cover many of the manufacturing defects in BiCMOS devices and that most open faults manifest themselves as delay faults. Analysis on the effects of bridging faults in BiCMOS is given in [10, 15, 16]. Reference [14] presents testability analysis and fault modeling of BiCMOS circuits in which the behavior of BiCMOS under faults is compared with CMOS. The most common type of BiCMOS circuits employ bipolar transistors to perform the functions of driving output loads and CMOS to perform logic functions.

Rapid advances, increasing complexities and shrinking device geometries in VLSI have enabled complex integrated circuits to be manufactured for extremely complex systems at lower costs. Various modes of failures can occur in complex VLSI devices, where bridging faults have been shown to be about half of the faults in CMOS circuits [17]. Another study [18], based on layout level defects using statistical data from fabrication process concludes that bridging faults can be up to 30% of all faults. Hence, bridging is an important failure mode which needs careful and systematic analysis. Bridging faults have long been regarded as a possible failure mode in digital systems [19, 20, 21]. Detailed examinations of bridging faults in nMOS/C莫斯 have been presented in [22, 23]. Bridging faults can occur within an integrated circuit or a printed circuit board during manufac-

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2 BiCMOS Devices

BiCMOS circuits employ one or two Bipolar Junction Transistors (BJTs) to perform the function of driving output loads and CMOS to perform logic functions. In this section, the operation of S-BJT Nand devices and its logic levels are presented.

2.1 S-BJT BiCMOS device

A Single BJT BiCMOS NAND realization is shown in Figure 1. The functioning of the BiCMOS NAND can be explained by first applying logic '0' to one or both of the inputs which would cause at least one P-device to be ON and at least one N-device in each serial N-pairs to be OFF. With the P-devices (P\textsubscript{1} and/or P\textsubscript{2}) ON, the base of the bipolar NPN transistor would be about 5V supplying base current and turning ON the bipolar transistor providing logic '1' at the output. With either of the inputs being at logic '0' and the other input at logic '1' would still cause either of the parallel connected P-devices to be ON and either of the series connected N-devices to be OFF. This would still supply base current to the bipolar transistor causing logic '1' at the output. With both the inputs at logic '1', the P-devices (P\textsubscript{1} and P\textsubscript{2}) would be turned OFF, and the N-devices N\textsubscript{1}, N\textsubscript{2}, N\textsubscript{3} and N\textsubscript{4} would be turned ON causing a conduction path from output node to ground. This will cause the output to be a logic '0'. Thus the circuit realizes the NAND function. Block diagram of a general S-BJT BiCMOS device is shown in Figure 2. An S-BJT BiCMOS gate consists of CMOS p- and n-pairs to perform logic function, and a BJT and a pull-down n-part for driving the output node. S-BJT BiCMOS devices do not have the full V\textsubscript{DD} to Ground logic swing of CMOS devices. The output High voltage (V\text{OH}) is limited to V\text{DD}-V\text{BR(QU)}. However, output Low voltage (V\text{OL}) is \approx 0V.

Major causes of bridging faults are related to the manufacturing defects. In the photolithography stages of the manufacturing process, diffusion and proximity are the prime source of excess metal causing bridging faults. Impurities and diffusion of metal are other sources responsible for such faults. Effects of input and output bridging faults in BiCMOS devices are examined for hard bridging as well as bridging with varying resistances. The following definitions are used in this chapter.

Definition 1: A Logic element is defined as a BiCMOS Gate (S-BJT or D-BJT) or a Complex BiCMOS Gate (S-BJT or D-BJT).

Definition 2: A Logical node is defined as a node where BiCMOS (S-BJT or D-BJT) logic levels are maintained, i.e., a node where specific voltage levels indicate logic levels '0' or '1'. In BiCMOS devices, input and output nodes are defined as logical nodes.

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3 Bridging Faults affecting only p or n-parts

In this section, we assume hard shorts for bridging faults under consideration, affecting only p or n-parts. An example of this class of bridging is shown in Figure 3. The three bridging faults (marked #1, #2 and #3) affect only the individual n-
Figure 3: A circuit example for bridging faults affecting only p or n-part.

part(1), n-part(2) or p-parts respectively. Bridging faults #1 and #2 affect non-logical nodes in n-part(1) only and bridging fault #3 affects non-logical nodes in p-part only for the logic element. The function realized by the example BiCMOS circuit is given as \( f = A \cdot B + C \cdot D \). However, for analysis of the bridging fault, a different approach is used to study the conduction paths in the n-part(1), n-part(2) and p-part. The input logic level and expression needed to turn the respective parts (n-part(1), n-part(2) and p-part) ON is obtained. For example, the expression for n-part(1) or n-part(2) to be turned ON in a fault-free gate is given as:

\[
f_{n,1,2} = A_1 \cdot B_1 + C_1 \cdot D_1.
\]

For n-part(1) and n-part(2), the input logic level that turn the n-transistors ON is logic ‘1’, hence, the suffix ‘1’ in the above expression for \( f_n \).

Similarly, for the p-part, input logic level ‘0’ turns the respective p-transistors ON, resulting in the following expression,

\[
f_p = A_0 \cdot C_0 + B_0 \cdot D_0 + A_0 \cdot D_0 + B_0 \cdot C_0.
\]

The Karnaugh Map for the fault-free complex BiCMOS gate is shown in Figure 4. The vectors which turn on the n-parts (1), (2) and p-part for the fault-free complex BiCMOS gate realizing the function \( f_n = A_1 \cdot B_1 + C_1 \cdot D_1 \) is shown in the Karnaugh Map. It can be seen that \( 1_n \) turns ON the n-part with logic level ‘1’ at the respective inputs and \( 0_p \) turns ON the p-part with logic level ‘0’ at the respective inputs.

Considering the bridging fault #1, which belongs to the class of bridging faults affecting only p- or n-parts (1) or (2). Bridging fault #1 affects only n-part(1). The expression for

Figure 4: Karnaugh Map for the fault-free example circuit.

Figure 5: Karnaugh Map for the faulty example circuit with bridging faults.
the n-part(1), n-part(2) and p-part under the above bridging faults #1 is given below:

\[ f_{n1} = A_1 \cdot B_1 + C_1 \cdot D_1 + A_1 \cdot D_1 + B_1 \cdot C_1 \] (Faulty)

\[ f_{n2} = A_1 \cdot B_1 + C_1 \cdot D_1 \] (Fault-free)

\[ f_{p1} = A_0 \cdot C_0 + B_0 \cdot D_0 + A_0 \cdot D_0 + B_0 \cdot C_0 \] (Fault-free)

In the above expressions, the superscript denotes the bridging fault under consideration and the subscript denotes the part [n-parts (1), (2) and p-part] which has the bridging fault. For example, \( f_{n2} \) denotes the expression for bridging fault #1 for fault in n-part(2). The vectors which turn on the n-part(1) is marked \( 1_n \) and the vectors which turn on p-part is marked \( 0_p \) for the complex BiCMOS gate under bridging fault #1 shown in Figure 5. Vector 1001 and 0110 corresponding to the Karnaugh map cells marked with \( 0_p/1_n \) causes both p-part and n-part to be ON. This results in a conduction path from \( V_{DD} \) to ground causing enhanced \( I_{DDQ} \) for the above vectors.

Similarly, the expression for the n-part(1), n-part(2) and p-part under bridging faults #2 and #3 are given below:

\[ f_{n2} = A_1 \cdot B_1 + D_1 \] (Faulty)

\[ f_{n2} = A_1 \cdot B_1 + C_1 \cdot D_1 \] (Fault-free)

\[ f_{p} = A_0 \cdot C_0 + B_0 \cdot D_0 + A_0 \cdot D_0 + B_0 \cdot C_0 \] (Fault-free)

\[ f_{n1} = A_1 \cdot B_1 + C_1 \cdot D_1 \] (Faulty)

\[ f_{n2} = A_1 \cdot B_1 + C_1 \cdot D_1 \] (Fault-free)

\[ f_{p} = C_0 + D_0 \] (Faulty)

The bridging faults in this class cause additional conduction paths to be created, resulting in enhanced \( I_{DDQ} \). Hence, bridging faults belonging to this class can be detected by \( I_{DDQ} \) monitoring schemes.

4 Input Bridging Faults affecting both p or n-parts

In this class of bridging faults, an input bridging fault affecting either n-part(1) or n-part(2) affects p-part or vice-versa. For example, the bridging fault #4 affecting n-part(1) also affects p-part. This fault (#4) causing inputs A and B to be bridged for n-part(1) also appears as a bridging fault for the p-part (#4’) as well as n-part(2). Hence, affecting both p-parts as well as n-parts. It may be noted that this class of bridging affects the logical nodes of the logic element.

Bridging faults of this class can be considered to be OR bridging or AND bridging. Let us first consider OR bridging between the affected inputs. For bridging fault #4, the expressions for OR bridging is given below:

\[ f_{n1}^{OR} = A_1 + B_1 + (C_1 \cdot D_1) \] (Faulty)

\[ f_{p}^{OR} = A_0 \cdot B_0 \cdot C_0 + A_0 \cdot B_0 \cdot D_0 \] (Faulty)

The expressions for both \( f_{n1}^{AND} \) and \( f_{p}^{AND} \) along with the Karnaugh map indicate that this fault can be detected at the logic level. The Karnaugh map does not show even a single cell where \( 1_n \) and \( 0_p \) overlap. Hence, does not cause enhanced \( I_{DDQ} \). However, gates connected at the input exhibit enhanced \( I_{DDQ} \) with opposite logic levels at the inputs [24], and can be detected by \( I_{DDQ} \) monitoring.

For bridging fault #4, the expressions for AND bridging is given below:

\[ f_{n1}^{AND} = A_1 \cdot B_1 + C_1 \cdot D_1 \]

\[ f_{p}^{AND} = (A_0 + B_0) \cdot C_0 + (A_0 + B_0) \cdot D_0 \]

\[ = (A_0 + B_0) \cdot C_0 + (A_0 + B_0) \cdot D_0 \]

The expressions for both \( f_{n1}^{AND} \) and \( f_{p}^{AND} \) along with Karnaugh map indicate that this fault cannot be detected at the logic level as the fault-free and faulty circuits provide the same expression. However, the gates connected at the input exhibit enhanced \( I_{DDQ} \) with opposite logic levels at the input. Hence, this class of bridging faults can be detected by \( I_{DDQ} \) monitoring. Figure 6 shows a bridging fault belonging to this class. By applying opposite logic levels to the gate inputs that are bridged (through output of gate G1 and G2), enhanced \( I_{DDQ} \) caused by the bridging fault can be detected.

Classification of input pattern are addressed in the next section.

5 Input Pattern Classification

In this section, we classify the input patterns according to the effect on the output in the presence of a fault. A section of the
BiCMOS gate [p-part, n-part(1) or n-part(2)] is either conducting or not conducting for a given vector. Let $P_t$ denote the set of vectors which turn ON the p-part. Similarly, let $N_{1t}$ and $N_{2t}$ denote the set of vectors which turn ON the n-part(1) and n-part(2) respectively. $N_{1t}$ and $N_{2t}$ are equivalent, and equal to the complement of $P_t$ as shown in Figure 7(a). $P_t'$, $N_{1t}'$ and $N_{2t}'$ are the set of vectors which turn ON the p-part, n-part(1) and n-part(2) respectively in the presence of fault $f$ in that part. An input vector, when applied to a fault-free BiCMOS gate causes a conduction path in the p-part($V_{DD}$ to output and base of bipolar) or in n-part(1)(base of bipolar to Ground) and n-part(2)(output to Ground). Here, we are considering irredundant gates such that, for each transistor there is at least one input vector for which all the conduction paths are through that transistor. This condition may not be true, for example, for high drive cells where many transistors with the same gate input are connected in parallel.

Below we give a series of lemmas that summarize the impact on the sets $P_t$, $N_{1t}$, $N_{2t}$ due to the different bridging faults.

**Lemma 1:** The set of vectors $(N_{1t})$ that cause the n-part(1) to turn ON in a BiCMOS gate is a proper subset of the set of vectors $(N_{1t}')$ that turn ON the n-part(1) in the presence of the bridging fault in n-part(1), i.e., $N_{1t} \subseteq N_{1t}'$.

**Proof:** Consider an input pattern $t \in N_{1t}$. As $N_{1t}$ is the set of vectors which makes the n-part(1) conduct, there is at least one conduction path through the n-part(1) for this vector. Consider an input pattern $t \in N_{1t}'$. As $f$ is a bridging fault causing an additional conduction path, the vector $t \in N_{1t}$ will also be a vector $t \in N_{1t}'$. Thus, if $t \in N_{1t}$, then $t \in N_{1t}'$.

Now, consider a vector $t' \in N_{1t}'$ which causes n-part(1) to provide a single conduction path due to the bridging fault. In the presence of the bridging fault, there will be a vector $t'$ such that an additional conduction path is created. This vector when applied to a fault-free circuit will not cause the additional conduction path. Thus, $t' \notin N_{1t}$. This completes the proof that $N_{1t} \subseteq N_{1t}'$. The resulting $N_{1t}$ region in the Venn diagram is shown in Figure 7(b). QED

**Lemma 2:** The set of vectors $(N_{2t})$ that cause the n-part(2) to turn ON in a BiCMOS gate is a proper subset of the set of vectors $(N_{2t}')$ that turn ON the n-part(2) in the presence of the bridging fault, i.e., $N_{2t} \subseteq N_{2t}'$.

**Lemma 3:** The set of vectors $(P_t)$ that cause the p-part to turn ON in a BiCMOS gate is a proper subset of the set of vectors that turn the p-part ON in the presence of the bridging fault $(P_t')$, i.e., $P_t \subseteq P_t'$.

The proof given for Lemma 4 can be easily extended for n-part(2) and p-part. The resulting $N_{2t}$ region and $P_t$ region in the Venn diagrams are shown in Figures 7(c) and (d) respectively.

**Theorem:** The set of vectors that cause the transistors in any part(n-part(1), n-part(2) or p-part) to turn ON in a BiCMOS gate under fault-free condition is a proper subset of the set of vectors that turn ON the corresponding part in the presence of a bridging fault.

The proof of this theorem follows from the above lemmas.

### 5.1 Test Sets for Bridging Fault Detection

With the above results, the test generation under bridging faults for BiCMOS devices can be done using the procedures given below. Since the manifestations of the bridging faults in the different blocks of p-part, n-part(1) and n-part(2) are known, appropriate test sets need to be generated to observe the manifestation of the respective faults at the output.

In the presence of a bridging fault, the size of the subset of vectors turning the corresponding conduction paths ON increases, resulting in the expansion of the corresponding regions in the Venn diagram. Based on this result, tests facilitating $I_{DDQ}$ testing for the various stuck-ON faults of a BiCMOS gate can be generated as given below.

- The set of test vectors for a bridging fault in the p-part is $(P_t \cap (N_{1t}))$.
- The set of test vectors for a bridging fault in the n-part(1) is $(N_{1t}' \cap P_t)$.
- The set of test vectors for a bridging fault in the n-part(2) is $(N_{2t}' \cap P_t)$.
- The set of test vectors for a bridging fault in the bipolar transistor is $(N_{1t} \cap (N_{2t}))$.  

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6 Conclusions

Bridging faults in single BJT BiCMOS devices were examined. Bridging faults within a transistor exhibits enhanced $I_{DDQ}$ and $I_{DDQ}$ monitoring can be used to detect such faults. Bridging faults affecting p- or n-parts also exhibit enhanced $I_{DDQ}$ and a pattern classification scheme was shown for SBJT BiCMOS gates. A methodology for generation of test sets in BiCMOS circuits using the above scheme was presented. The test sets obtained can be used for detecting the various bridging faults that occur in BiCMOS devices.

References