Abstract

The Generalized Recognition Of Gates is an innovative and technology independent tool of abstraction. It translates any VLSI or ASIC microelectronic circuit from its netlist format into both VHDL and VERILOG descriptions which express its behavior. The CMOS, NMOS, Bipolar and BiCMOS technologies can all be handled. One of the most important characteristics of the tool is that it is driven by an external library of rules. This reverse engineering approach is fast and well adapted to both the verification and the technology migration tasks.

Principles

The abstraction tool is flexible enough to process any full custom, standard cell or gate array style of design as it is based upon pattern matching mechanisms. These mechanisms are controlled by an external and user defined library of rules which can easily be enhanced and updated. Each rule encapsulates a parametrized model of a gate and defines precisely the VHDL and VERILOG behavior one wants to get. As soon as components are filtered by the model of a circuit, they are replaced by a surrounding entity. Complexity can be easily managed in a hierarchical manner since these entities may be referenced in higher level models. Recognition of gates with a variable number of items is allowed thanks to a kind of recursivity. Built-in functions can automatically recognize the CMOS usual gates. The tool is autonomous as there is no need to interact with it once it has been launched. A graphical interface allows to interrogate the ending result of the abstraction and to locate the recognized gates along with their behavior. This contributes to make the product more user-friendly.

Applications

- Verification: with functional abstraction, one can check that the physical gate level realization matches the higher level model by simulation or formal proof.
- Technology migration: re-implementing an old design into a more recent technology is easy when entering its abstracted behavior into a synthesis tool. All or part of old designs coming from different technologies such as NMOS CMOS, Bipolar or BiCMOS, can easily be retargeted and modified. By using a selected vendor’s specific library, one can optimize the new design for the target technology and specify its new timing requirements. Performance and improvements can be gained in return, design time and money can be saved.

Results

The principles are now well proven, since they have been in active use for several years in BULL S.A.. The tool is proved reliable and efficient, and it has been tested successfully in other companies.

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