Fast Computation of Substrate Resistances in Large Circuits

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Abstract

In this paper, we describe a method to quickly and accurately estimate substrate coupling effects in analog and mixed digital/analog integrated circuits. Unlike numerical methods, that can be used for circuits containing only a few hundreds of substrate terminals, the new method can quickly extract circuits containing many thousands of substrate terminals. Examples are given that show that the method is sufficiently accurate for practical circuit verification. The method has been implemented in the layout-to-circuit extractor Space.

1 Introduction

In modern analog circuits and mixed digital/analog circuits, coupling effects via the substrate can be an important cause of malfunctioning of the circuit. This problem becomes more prominent as (1) there is a trend to integrate more and more different components on a chip, (2) the decrease of wire width and increase of wire length causes the interconnect parasitics and hence the level of noise on the chip to increase, and (3) the use of lower supply voltages makes the circuits more sensitive to internal potential variations.

The substrate coupling effects in integrated circuits can be verified by computing the substrate resistances between all circuits parts that inject noise into the substrate and/or that are sensitive to it. The noise injectors are mainly the contacts that connect the substrate and the wells to the supply voltages. The current variations in the supply lines cause fluctuating potentials over their resistances and inductances, that are injected into the substrate via the substrate contacts and the well contacts. The noise receivers are often the bulk connections of the transistors. Other parts that may generate noise and/or that are sensitive to it are (1) drain/source areas of transistors, (2) on-chip resistors and capacitors, and (3) interconnect wires that are coupled to the substrate via a (large) substrate capacitance. In the following, we will call the parts of the circuit that generate noise and/or that are sensitive to it, the *substrate terminals* of the circuit.

Several publications already describe how substrate coupling effects can be verified prior to the fabrication of the circuit. In [1] and [2], a 2D device simulator is used to simulate the substrate coupling effects. This method allows to investigate the general effects of guard-rings, substrate contacts, etc., but it is not well suited for practical circuit design. More general methods, that generate a 3D mesh for the substrate to determine the coupling effects, are described in e.g. [3] and [4]. Methods that use a 3D boundary-element method and that generate much fewer elements are found in [5, 6] and [7]. However, because of high memory usage and long computation times, these numerical methods do not handle circuits containing more than a few hundreds of substrate terminals.

Although the numerical methods that are mentioned above can advantageously be used to verify small circuits or local effects in large circuits, in practice, substrate coupling effects often occur for relatively large circuits. Hence there is a need for methods that can quickly estimate substrate resistances for large circuits. Attempts to speed-up the computation of substrate resistances are found in [8] and [9]. In [8], parameterized lumped models are given for several different isolation schemes using guard-rings. In [9], the speed-up is obtained by precomputing point-to-point impedances, which are then used to find the admittance matrix for the actual terminal configuration. Also hierarchy and delimitation are used in [9] to reduce computation complexity. However, the latter method still requires matrix inversion.

In this paper, we describe a new method for substrate resistance computation that is simple, fast and general, and that has moreover been implemented in a layout-to-circuit extractor to extract the substrate resistances in combination with the rest of the circuit, including interconnect parasitics. The output of the extractor can directly be verified, e.g. using a circuit simulator.

To simplify the computation of the substrate resistances and to reduce the complexity of the output circuit, the method uses the notion of a “substrate node” to which all substrate terminals are connected via a resistance. Direct coupling resistances between substrate terminals are only computed between terminals that are “neighbors” of each

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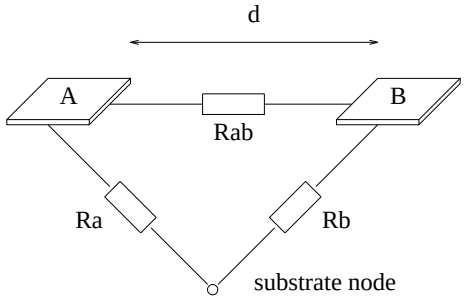

Figure 1: *Substrate model for a configuration with two substrate terminals.*

other. Whether or not two terminals are considered neighbors is determined by a Delaunay triangulation of the area between the terminals. The speed-up is further obtained by using interpolation techniques in combination with results for standard terminal configurations.

We compare the new method with a numerical method and show that the method is sufficiently accurate for practical circuit verification. We also show that the method can quickly extract circuits containing many thousands of substrate terminals.

The structure of this paper is as follows. First, in Section 2, we describe the model that is used to compute substrate resistances. Next, in Section 3, we discuss the selection of the terminal pairs for which direct coupling resistances are computed. Then, in Section 4, we describe the computation of the values of the substrate resistances. In Section 5, we present results of the method. Finally, in Section 6, we give a discussion.

2 The Substrate Model

The substrate model that we use to compute the substrate resistances is illustrated in Figure 1. The figure shows two rectangular substrate terminals, representing substrate contacts or transistor bulk connections, etc.

In the substrate model, we define a common substrate node to which all substrate terminals are directly connected via a resistance. For example, in Figure 1, terminal A is connected to the substrate node via resistance R_a, and terminal B is connected to the substrate node via resistance R_b. The substrate node is identical to the reference node or ground node that is found with the boundary-element method [5–7]. Usually the substrate node can be assumed to be present at infinity. However, for substrates that have a well-conducting bottom layer or a metal backplane, the substrate node accurately represents this part of the circuit [1].

The value of the resistance between a terminal and the substrate node is primarily determined by the properties of the substrate and the geometry of the terminal.

In the substrate model, a resistance is also computed between terminals that are "neighbors" of each other (see Section 3 for the definition of "neighbor" terminals). In Figure 1, such a direct coupling resistance has been computed for terminal A and terminal B and is called R_{ab}. The direct coupling resistance between two terminals carries the current between those terminals that is not flowing via the substrate node. Its value is dependent on the properties of the substrate, on the geometries of the terminals and on the position of the terminals with respect to each other. The value of the direct coupling resistance is large if the terminals are far apart and it becomes smaller when the distance between the terminals becomes smaller.

To demonstrate the validity of the above substrate model, we consider the configuration that is shown in Figure 2. It consists of a heavily doped substrate of 300µ (resistivity 0.05 Ω·cm) with a lightly doped epitaxial layer of 7µ (resistivity 15 Ω·cm) grown on it. The dimensions of the substrate and the epi-layer in horizontal directions are considered infinite. On top of the epi-layer there are two terminals of size $W \times W$ that are at a distance d. Substrate resistances have been computed for this configuration using the 3D substrate resistance computation program described in [7].

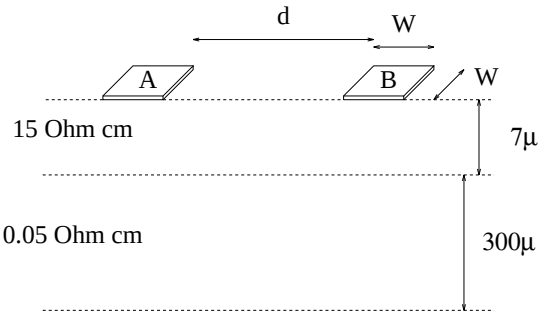

Figure 2: *Heavily doped substrate with a lightly doped epi-layer and two terminals.*

In Figure 3, the resistance between the two terminals in Figure 2 is shown as a function of their distance, for different sizes of the terminals. From the results we note that the resistance between the terminals approaches an asymptotic value — depending on the geometry of the terminals — as the distance between the terminals is increased. This can be explained by the fact that when the distance between the terminals is large compared to the thickness of the epi-layer, almost the complete current between the terminals will flow via the well-conducting bottom layer (see also [1]). The total resistance is then primarily determined by the resistance between terminal A and the bottom layer, and the resistance between terminal B and the bottom layer, which correspond to respectively resistance R_a and resistance R_b in the model in Figure 1.

When the distance d becomes smaller, the total resistance between terminal A and terminal B is more and more determined by the resistance of that part of the epi-layer that is between terminal A and terminal B. This resistance is represented in Figure 1 by the resistance R_{ab}.

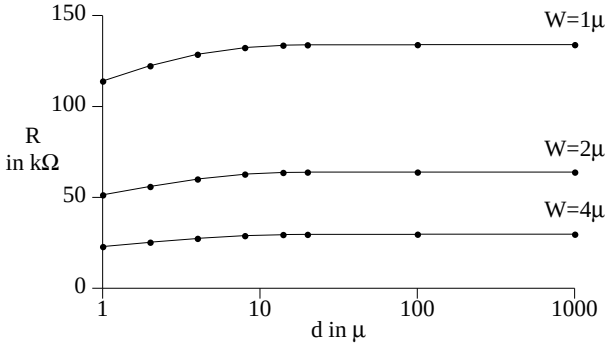

Figure 3: *Resistance between the two terminals in Figure 2 as a function of their distance d, for different terminal sizes.*

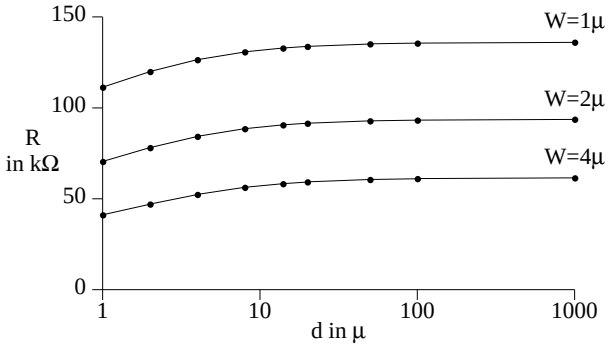

Figure 4: *Resistance between two terminals on top of a* 300μ *thick lightly doped substrate (resistivity 15* Ω·*cm) as a function of their distance d, for different terminal sizes.*

Although the validity of the model in Figure 1 is intuitively verified for substrates with a well-conducting bottom layer as shown in Figure 2, it appears that the model can also be used for other types of substrates. This is illustrated in Figure 4 by computing the resistance between two terminals on top of a substrate that is similar to the first type but that has no epi-layer and consists of only a 300μ thick lightly doped substrate (resistivity 15 Ω·cm). The results show a similar behavior as in Figure 3. The results in Figure 4 are confirmed by theoretical work that shows that the resistance between two terminals on top of a conducting half-space, for distances much larger than the sizes of the contacts, is independent of the distance between the contacts (see [10]).

3 Network Reduction

When N is the number of substrate terminals and when a direct coupling resistance is computed for each pair of substrate terminals, the total number of direct coupling resistances is $\frac{1}{2}N(N-1)$. For large circuits, this number can become very large. This not only results in long computation times, but also in a large output network. However, many coupling resistances between terminals that are far apart are large compared to the total resistance along parallel paths via other terminals and/or via the substrate node (see the previous section). Therefore it is advantageous to omit these resistances.

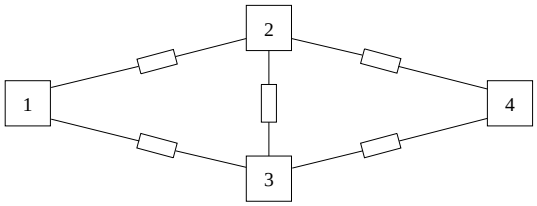

Figure 5: *The direct coupling resistance between terminal 1 and 4 is not computed because of the presence of the resistance paths via terminal 2 and 3.*

In [9], a delimitation process is used in which a coupling resistance between two terminals is only computed if there exists a path in the layout between them that is not obstructed by another terminal (or by a predefined maximum number of other terminals). This strategy is useful for guard-rings, but it is not very efficient for circuits where many small contacts are present. This is illustrated in Figure 5. In Figure 5, there is a path in the layout between terminal 1 and 4 but it is not necessary to compute the (large) resistance between these terminals because this resistance is shunted by the (smaller) total resistance of the paths via terminal 2 and 3.

Therefore, to select the terminal pairs for which direct coupling resistances are computed, we use a method that first constructs a Delaunay triangulation of the set of terminals. A Delaunay triangulation is a planar graph that is defined as the dual of a Voronoi diagram [11]. Given a set of points, the Voronoi polygon of one point is defined to be the set of all points in the plane closer to the given point than any other point in the point set (see e.g. [12, pages 366–368]). The union of all the Voronoi polygons for a point set is called its Voronoi diagram. The Delaunay triangulation is then the set of lines that are drawn between each pair of points of which the Voronoi polygons are adjacent. Clearly, in the Delaunay triangulation, a line exists between two points if they are “neighbors”. Hence, the presence of such a line forms a good criterion to determine that a direct coupling resistance between these terminals is computed.

In [11], an algorithm has been described to iteratively create a Delaunay triangulation of a finite set of points that, apart from a presorting step, runs in almost linear time. Because of the iterative construction of the diagram, the algorithm is easily implemented in a scanline based [13] layout-to-circuit extraction program [14].

We have adapted the algorithm described in [11] to our situation by taking the corners of the terminals as the point set and by requiring that the Delaunay edges do not intersect the terminal boundaries. A direct coupling resistance between two terminals is computed if, and only if, there is at least one line of the Delaunay triangulation that directly connects the terminals. An example of a Delaunay triangulation for a set of terminals is given in Figure 6.

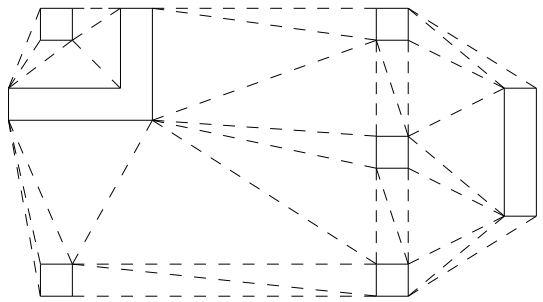

Figure 6: *Example of a Delaunay triangulation. The terminals are drawn in solid lines. A direct coupling resistance is computed between two terminals if there is at least one line of the Delaunay triangulation that directly connects them.*

If we consider the Delaunay triangulation as a graph in which the terminals are the nodes of the graph and there is an edge whenever there is at least one line connecting the terminals, then the number of resistances in the output network can be increased by computing a direct coupling resistance between each pair of terminals if the terminals are at a distance $\leq L$ in the corresponding graph.

4 Resistance Computation

The values of the resistances in the substrate model are computed via interpolation between known resistance values for some standard configurations. The resistance values for the standard configurations can be obtained via measurement on real circuits or — as we did — by using a numerical method [7].

In Figure 7.a, the value of the conductance between a terminal and the substrate node is shown as function of the area of the terminal for a homogeneous substrate. In Figure 7.b, the value of the same conductance is shown as a function of the perimeter of the terminal. Note that in both cases there is (approximately) a linear dependency between the conductance and the area or the perimeter. Therefore, for the resistance between a terminal and the substrate node, the following interpolation formula is used (see also [1])

$$R_{sub} = \frac{1}{G_{sub}} = \frac{1}{k_1 + k_2 P + k_3 A}, \qquad (1)$$

where P is the perimeter of the terminal, A is the area of the terminal, and k_1, k_2 and k_3 are empirical fitting parameters that are obtained from the resistance values of at least 3 different configurations.

The direct coupling resistance between two terminals as a function of the distance between the terminals, for different terminal geometries, is plotted in Figure 8. Based also on other experiments, we have found that a reasonable value for the direct coupling resistance between two terminals is obtained via the interpolation formula

$$R_{dir} = \frac{K d^p}{\sqrt{A_a} + \sqrt{A_b}}, \qquad (2)$$

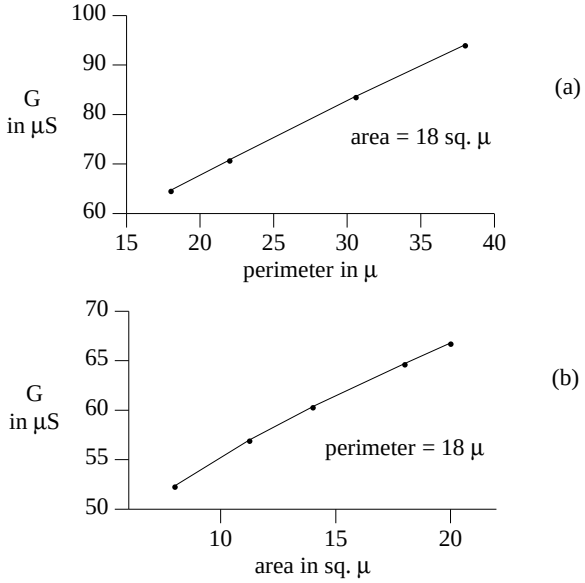

Figure 7: *(a) Conductance to substrate as a function of the terminal perimeter. (b) Conductance to substrate as a function of the terminal area.*

where A_a and A_b are the areas of the terminals, d is the minimum distance between the terminals and p and K are empirical fitting parameters (e.g. in Figure 8, $p \approx 0.8$)

When the distance between two terminals is decreased, a part of the current between the terminals that normally flows via the substrate node will flow via the direct coupling resistance. This is modeled by subtracting an (empirically determined) fraction of the total direct coupling conductance that is connected to a terminal from the conductance between that terminal and the substrate node.

5 Results

The substrate resistance computation method has been implemented in the layout-to-circuit extractor Space [14]. Space can extract from a layout description the active devices, the interconnect parasitics and the substrate resistances, using this method or the method described in [7].

To obtain information about the accuracy of the method, results of the new method have been compared against results of the method in [7]. Substrate resistances have been computed for two different terminal configurations on top of two different types of substrates. Top views of the terminal configurations are shown in Figure 9. The types of substrates that are considered are the same as in Section 2.

The results are shown in Table 1 and Table 2. To make it easier to compare the different results, the substrate node has been removed from each network via Gaussian elimination. From the results we see that for small resistances — which are the most important ones — the error is not larger than 10 %. We also see that the accuracy of the method is somewhat better for substrates with an epi-layer and a well-

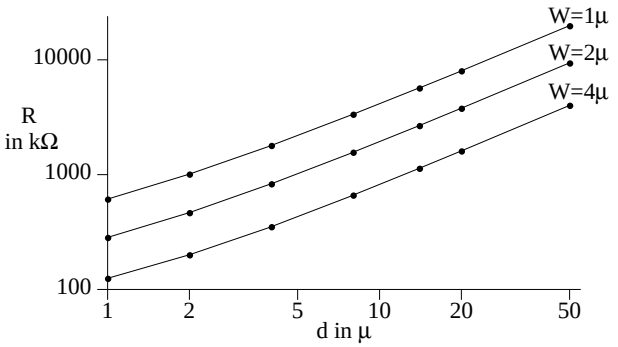

Figure 8: *Direct coupling resistance between two terminals as a function of the distance.*

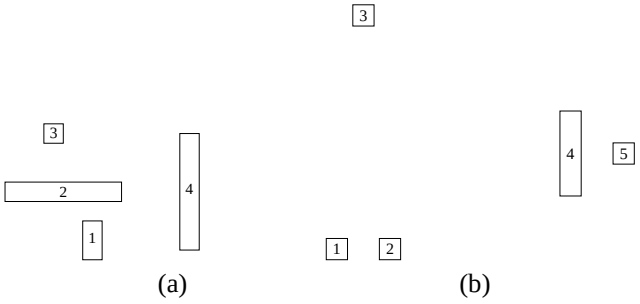

Figure 9: *(a) Terminal configuration 1. (b) Terminal configuration 2.*

Table 1: *Resistances (in kΩ) for the terminal configuration in Figure 9.a on a heavily doped substrate with epi-layer (lay. = 2) and on a lightly doped substrate (lay. = 1). BEM = method in [7], interp. = method in this paper.*

lay.		R_{12}	R_{13}	R_{14}	R_{23}	R_{24}	R_{34}
2	BEM	85.4	516	126	136	53.6	197
	interp.	90.1	560	120	144	48.7	180
	% diff.	5.5	8.5	-4.8	5.8	-9.1	-8.6
1	BEM	85.6	526	129	136	54.4	202
	interp.	90.8	661	121	143	50.7	178
	% diff.	6.1	25.7	-6.2	5.1	-6.8	-11.9

Table 2: *As in Table 1 but now for the terminal configuration in Figure 9.b*

lay.		R_{12}	R_{13}	R_{14}	R_{15}	R_{23}	R_{24}	R_{25}	R_{34}	R_{35}	R_{45}
2	BEM	263	412	191	530	418	188	531	172	480	123
	interp.	270	421	185	512	429	179	523	164	472	129
	% diff.	2.7	2.2	-3.1	-3.4	2.6	-4.8	-1.5	-4.7	-1.7	4.8
1	BEM	259	412	197	552	422	191	548	176	495	122
	interp.	258	396	202	547	418	182	586	167	519	126
	% diff.	-0.4	-3.9	2.5	-0.9	-0.9	-4.7	6.9	-5.1	4.8	3.3

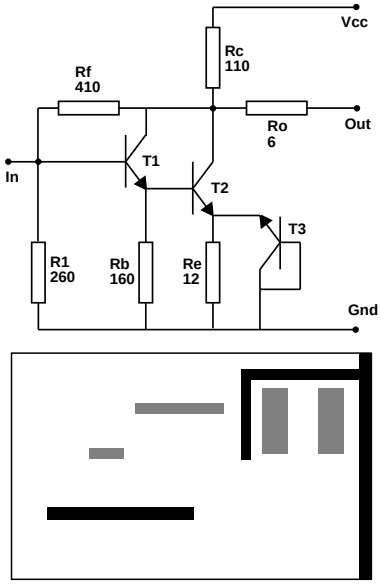

Figure 10: *Schematic (a) and simplified layout (b) of a bipolar amplifier. Grey areas indicate the position of a transistor (from left to right T1, T2, T3a and T3b), black areas indicate the position of a substrate contact.*

conducting bottom layer than for homogeneous substrates. This is because with a well-conducting bottom layer the conductance to the substrate node is more dominant compared to the coupling conductances and hence the error that is made by independently computing the coupling conductances is less important.

Another example is shown in Figure 10. We study the high frequency behavior of a bipolar amplifier on a substrate consisting of a 1.4μ 0.15Ω·cm top layer and a 300μ 4Ω·cm bottom layer. The circuit in Figure 10 was extracted without substrate resistances, using the substrate resistance computation method in [7] and using the method described in this paper. In all cases, the resulting circuit was simulated using Spice. The simulation results are presented in Figure 11. They show that the substrate coupling effects that are estimated using the new method are almost identical to the results that are obtained using the method in [7].

On an HP 9000/735 computer, extraction of the amplifier, using the method in [7], took 3 minutes and 4 seconds (248 elements were used). Extraction on the same computer, using the new method, took less than 1 second. More performance figures for the new substrate resistance extraction method are presented in Table 3.

6 Discussion

In this paper, we have described a method to quickly compute accurate substrate resistances for large circuits. Problems that are caused by substrate coupling are usually global problems that require the simulation of the complete circuit in order to uncover them. Therefore, we have aimed at

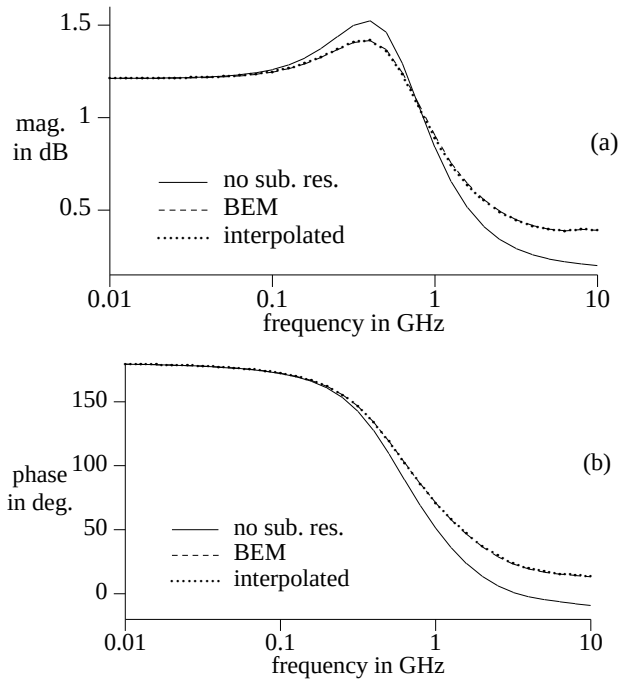

Figure 11: *Simulated magnitude (a) and phase (b) of the transfer functions of the amplifier vs. frequency.*

the development of a method that computes in a reasonable amount of time all relevant substrate resistances of a complete circuit.

To efficiently compute the substrate resistances, the method uses the notion of a (virtual) substrate node to which all substrate terminals are connected. It computes direct coupling resistances only between substrate terminals that are close to each other. Note that this model is more or less similar to the model that is used to compute capacitances using an area/perimeter method: The substrate node in the substrate resistance model is equivalent to the ground node in the capacitance model and, in analogy to the coupling capacitances between wires in the capacitance model, direct coupling resistances between substrate terminals are only computed between neighbor terminals.

Because of the speed of extraction method, the circuit simulation that is performed afterwards will, in general, require much more time than the computation of the substrate resistances. Hence, it becomes more and more important to investigate other verification techniques that can be used in combination with the method for fast substrate resistance extraction.

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Table 3: *Total extraction times (on an HP 9000/735) for circuits having different numbers of substrate terminals.*

circuit	nr. tors	nr. sub. term.	cpu time (in sec.)
pla	328	418	6.4
processor	1467	1357	27.7
memory	6360	7057	320.1

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