"I_{DDQ}: You heard the Hype, but what’s really coming?"

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1 I_{DDQ} Testing

I_{DDQ} testing is as old as CMOS IC technology itself. In the last 20 years various companies have been successful in using I_{DDQ} testing where applications demanded high quality and high reliability ICs, while many others have failed. Failure to be successful with I_{DDQ} has many causes, it is too slow for production testing, the yield loss too great, ICs are leaking too much current, the process is too leaky, nobody can select the vectors. I_{DDQ} testing has never broken through into the mainstream of IC testing for many reasons. Is this going to happen in 1996? Or is this just another cyclical re-appearance of an old idea?

The best evidence to support the idea of a radical change in I_{DDQ} testing is the strong interest in the USA industry, especially in the semiconductor and automotive industries. Evidence that I_{DDQ} testing is being taken seriously are common place, in conferences and workshops. Intel reports using the method for 80386 in laptop applications. Intel also tried to make the P6 I_{DDQ} testable, but that was too much of a challenge. This year the US automotive industry made a significant step in accepting I_{DDQ} testing by allowing vendors to trade-off I_{DDQ} vectors against stuck-at fault coverage in a new draft quality standard, CDF-AEC-Q100. This is a market where the European semiconductor vendors have retained a strong role, so this is an important step for the IC industry in Europe.

Nevertheless, this begs a further question, why is the US automotive industry pushing the semiconductor industry, not the European automotive industry? Again it would seem that European industry can only react to external events, there are no plans in Europe, no roadmaps for the customer or vendor to follow. Without these roadmaps it is difficult to judge what the position of the European industry is and where it will be in a few years. This hot-topic session allows some major players in the European IC industry to reveal their plans for the future of I_{DDQ} testing.

The remainder of this paper discusses the status of the US industry roadmaps as issued by the SIA and examines the USA automotive industries input to the discussion through the draft CDF-AEC-100 standard on fault simulation.

1.1 Content of the Roadmaps

Technology roadmaps for I_{DDQ} testing need to address six basic areas:

1. Instrumentation for I_{DDQ} measurement
2. CAD tools
3. Fault Models and Metrics
4. I_{DDQ} testable ICs and libraries
5. Diagnostic tools
6. Quality Function Deployment (TQM)

Each of these areas should be developed to ensure the successful introduction of I_{DDQ} testing.

Instrumentation for I_{DDQ} testing is needed to allow the IC test department to make this form of testing economically viable on the current ATE. CAD tools are needed to allow I_{DDQ} vectors to be selected on a scientific basis, not a random selection of vectors by the test engineer. To implement CAD tools the industry needs to adopt a common set of fault models for I_{DDQ} test generation or fault simulation. While the fault metrics are needed to allow different forms of fault coverage to be evaluated in a common framework to allow the test vectors from the design department to be approved for production. At the same time the design department must ensure that ICs and cell libraries are I_{DDQ} testable, if not the value of I_{DDQ} testing is totally lost. The commitment to I_{DDQ} testing from the design managers must be formal-
ized. \texttt{I_{DDQ}} testing has a significant disadvantage, but one that can be turned into an advantage. \texttt{I_{DDQ}} is too effective in detecting defective ICs, even parts with minor failures of dielectrics will be identified. This can lead to unacceptable yield loss, the solution to this problem is to provide good diagnostic feedback to the fab. This requires investment in diagnostic tools that allow systematic problems in the process such as weak gate-oxides, poor dielectric in the back-end, and particle contamination sources to be identified. Once known they can be include in a PDCA (Plan-Do-Check-Action) programme to improve the yield. Finally management commitment to the project must be clearly present (TQM), otherwise the take-up across the company will be weak.

"The simple stuck-at fault models need to be supplemented by models for static current test (\texttt{I_{DDQ}}) faults, as well as bridge faults..."

"\texttt{I_{DDQ}} is a technique for measuring the quality of an IC..."

"The traditional technique of externally applying millions of vectors must give way to increasing use of BIST, DFT and \texttt{I_{DDQ}} testing."

"The use of techniques such as \texttt{I_{DDQ}} testing or wafer level burn-in should be explored with some urgency."

2 SIA Roadmaps: Fault Models & \texttt{I_{DDQ}} Test

Last year the Semiconductor Industry Association (SIA) released its National Technology Roadmaps for Semiconductors. In this document an attempt has been made to define trends in the test technology area in a rigorous fashion. Originally introduced in 1992 this updated version of the roadmaps was released in 1995 with a much broader focus on design and test. Because of the dominant position of the US in semiconductors, this roadmap can be seen as an international roadmap thus very influential on the worldwide electronics industry.

In the test technology parts of the roadmaps it can be seen that the general approach of defect oriented testing at block and IC level using \texttt{I_{DDQ}} testing combined with voltage is supported. The classes of faults/defects presented in the SIA roadmap are similar to those proposed by Sandia Labs in a paper at the ITC in 1994. However, this SIA roadmap is with a timetable (see page 35 of SIA Roadmaps). So, for example, the following years have been planned for earliest introduction of new fault model across the industry:

- 1998: Leakage fault models
- 1999: Bridge fault models

In general the SIA road maps are very positive on the value of \texttt{I_{DDQ}} testing as seen from the following quotes.

2.1 Europe's Reaction to SIA Road Maps

There is a clear strategy and urgency in the SIA roadmaps for \texttt{I_{DDQ}} testing, however, Europeans can only speculate on how the US semiconductor companies plan, for example, to define the leakage or bridge fault models for industry-wide use. Many of the joint activities of the US industry are not open to external companies either Japanese or European, even if they have significant investment in the US industry. If European companies wish to gain access to results from industrial studies under taken by US based consortia they need to barter with similar results.

However, European companies have little or no role in this debate. A debate that will probably influence the EDA community quite strongly.

2.2 An open problem

One minor problem area foreseen in the SIA 1995 roadmaps by Philips, among others, is the uncertainty on the position of open defects and corresponding open fault models. It is true that for good reasons open defects are not a major yield or PPM problem for the industry in general. However, open defects are a problem in rogue lots and the potential problems of open defects in very deep sub-micron technologies (< 0.2 \(\mu\)m) remains. We would therefore foresee that fault models for opens should be planned for the period 2005-2007 in the next series of SIA roadmaps. Perhaps this is an area of research that European industry could play a role in?
3 US Automotive Industry: CDF-AEC

At present the only open forum for this debate seems to be the Chrysler Delco Ford - Automotive Electronics Council (CDF-AEC). CDF-AEC is a good model for the discussions between the semiconductor industry and its customers to agree a basis for future fault models and \textit{ IDDQ} testing. CDF-AEC have recently issued a draft standard (CDF-AEC-Q100) for fault simulation of IC in automotive products. This standard would allow a vendor to aim for a lower stuck-at fault target of 95%, if ten or more \textit{ IDDQ} vectors are employed. Without \textit{ IDDQ} vectors the vendor would have to demonstrate 98% stuck-at fault coverage, and indicate why the coverage was less than 100%. This is a big incentive to the design department to make \textit{ IDDQ} testable ICs.

CDF-AEC offers an open forum for discussions between customer and vendor. A degree of openness is needed in this debate to allow other customers to participate and for the supporting industries, such as EDA vendors, to plan product development, again another important part of roadmaps.

4 Bibliography
