RC-Interconnect Macromodels for Timing Simulation*

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ABSTRACT

Most timing simulators obtain their efficiency over circuit simulation in terms of explicit integration algorithms that have difficulty handling the stiff RC circuit models which characterize interconnect-dominated paths. In this paper we describe a reduced-order N-port interconnect macromodel for timing simulation. This macromodel is shown to improve the timing simulation efficiency dramatically since it alleviates the stiff circuit problem. Moreover, through its compatibility with the simple timing simulation transistor models, it is shown that this macromodel does not suffer from the dramatic increase in complexity with an increase in the number of ports like circuit simulation.

I. INTRODUCTION

Timing simulators [1,2,3,4,5] have filled the gap between accurate, inefficient, circuit simulators such as SPICE [6] and, efficient, yet delay independent, functional logic simulators. Timing simulators often obtain their efficiency over circuit simulation using some form of explicit numerical integration for nonlinear transient analysis. ELogic [2] (represented by the ELogic-1 algorithm) and SPECS [3], for example, both employ simple device models and clever explicit integration schemes.

All explicit integration schemes struggle with the analysis of stiff circuits -- circuits with time constants spread over a large range of magnitudes. RC interconnect circuits are problematic for most timing simulation algorithms for this reason. Even ILLIADS [4], which solves for the node voltages analytically, does not inherently handle linear resistors between nodes. It is therefore desirable to generate reduced-order interconnect macromodels to avoid the stiff system problem.

Asymptotic Waveform Evaluation (AWE) [7] has been successfully applied for generating reduced order transfer and driving-point admittance models for RLC interconnects. With AWE, it has been demonstrated that dominant time-constant N-port macromodels can be constructed and imbedded into circuit simulators [8,9]. ACES, a timing simulator with piecewise linear (PWL) device models, also employs an N-port AWE macromodel [5] similar to that in [9]. But typical explicit integration simulators, such as ELogic and SPECS, are incompatible with these N-port macromodels because of their piecewise constant voltage and current restrictions respectively.

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In this paper we propose an efficient AWE-based interconnect macromodel for SPECS and ELogic type simulators. Moreover, it will be shown that interconnect macromodels with a large number of ports (like a clock tree with multiple nonlinear drivers and loads) are evaluated with less computational complexity using simple device models like those used in SPECS, as compared to those used in SPICE or a PWL simulator.

This paper is structured as follows: Section II reviews the explicit integration based timing simulation algorithms of SPECS and ELogic, and provides a brief overview of general N-port theory. The implementation of interconnect macromodels in SPECS is described in Section III, followed by results in Section IV and our conclusions in Section V.

II. BACKGROUND

II.1 SPECS and ELogic Like Algorithms

SPECS, as described in [3], is a timing simulator that uses piecewise constant i-v characteristics to model all dissipative circuit components (including the linear resistors). It computes the time required by a device variable to reach a new region. It employs both temporal and spatial latency through event-driven methods and circuit partitioning. The strength of SPECS is given by the simple integration scheme, that is equivalent with forward Euler, but with reliable stability control.

The SPECS modeling approach also yields piecewise constant currents through all branches, and piecewise linear voltages at all nodes. Furthermore, there is a requirement for a capacitor from every node to the ground, which is not considered an unreasonable assumption for MOS circuits. Considering a node k to which both linear and nonlinear dissipative elements are connected, the equivalent circuit shown in Fig. 1 can always be constructed in SPECS. SPECS can be used effectively for large digital MOS circuits, with more than 60x speed-up while keeping the average error under 5% as compared with SPICE.

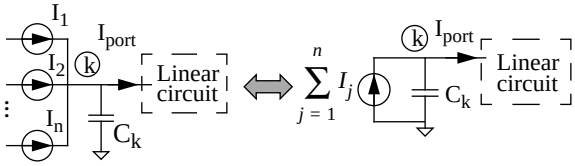

Fig. 1 Equivalent node circuit for SPECS. I_j with j=1,n are current sources modeling nonlinear devices. C_k is the total capacitance of node k.

ELogic, as described in [2], defines a set of discrete (not necessarily uniform) states of the node voltages. The event scheme captures the transition times between adjacent states (node voltages generate events), with the unknown being the time interval up to the next node voltage transition. In contrast to SPECS, the linear resistor is a basic modelling component in ELogic.

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The MOS transistor is modeled by a small signal resistor in ELogic, sometimes in parallel with a current source. The model parameters (resistor and current source values) are updated at each event. A grounded capacitor from each node is required.

The integration schemes in various versions of ELogic are different, but the ELogic-1 algorithm (the fastest but also requiring the biggest number of intermediate states for a given accuracy) uses forward Euler. The equivalent circuit for a generic circuit node is given in Fig. 2.

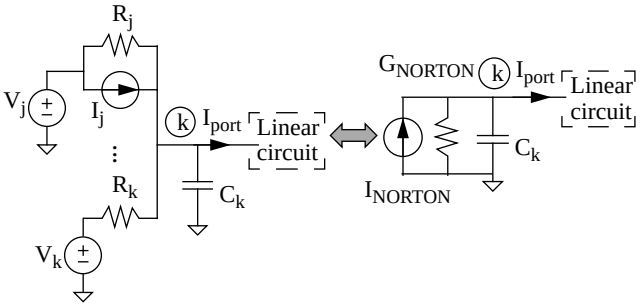

Fig. 2 Equivalent circuit for ELogic. I_j is part of nonlinear device model. R_j and R_k represent the nonlinear devices. C_k is the total capacitance of node k.

The macromodels we are proposing will work equally well in SPECS, ELogic-1, or any similar explicit-integration based timing simulator tool. But for demonstration purposes, we will apply them in the commercial version of SPECS, SPECsim[1].

II.2 N-port Models

A circuit that contains only linear, time invariant elements can be represented by a set of N linear relations between the voltages and the currents at N selected ports. The state of the multi-port can be uniquely specified by either all of the voltages (*y*-parameters), all of the currents (*z*-parameters), or a combination of currents and voltages (hybrid parameters) at the ports [10].

In SPECS, at each node there will be multiple current sources that can be represented by their combined sum, and a single capacitor to ground. If we include the linear capacitor to ground as part of the interconnect macromodel, then each port of the macromodel sees only a current source. This permits a very efficient representation of the problem in terms of *z* parameters.

At the k-th port of an N-port macromodel, the *z* parameter equation expresses the voltage at that port in terms of the currents at all of the other ports:

$$v_k = z_{k1} i_1 + z_{k2} i_2 + \ldots + z_{kN} i_N \tag{1}$$

The k-th port equation in (1) can be also be written as:

$$i_k = \frac{v_k}{z_{kk}} - \frac{z_{k1}}{z_{kk}} i_1 - \ldots - \frac{z_{k,k-1}}{z_{kk}} i_{k-1} - \frac{z_{k,k+1}}{z_{kk}} i_{k+1} - \ldots - \frac{z_{kN}}{z_{kk}} i_N = \frac{v_k}{z_{kk}} - \sum_{\substack{j=1 \\ j \neq k}}^{n} f_{kj} \cdot i_j \tag{2}$$

which is easily implemented as an N-port macromodel in terms of linear circuit components.

In general, we would compute the multiport parameters for the interconnect circuits without considering the elements at the ports that are driving the interconnect. But for this SPECS implementation, we will show that we can obtain the utmost efficiency if we include all of the capacitors to ground into the macromodel such that the ports are driven only by the independent current sources that represent the MOSFETs. We can update the macromodel parameters when capacitors are changed or added during a design optimization loop (gate resizing).

III. N-PORT MACROMODEL IMPLEMENTATION

In the most general case, if we decide to use the *z*-parameter description of the N-port in a timing simulator, (equivalent implementations are possible for the *y*-parameter description), we may want to directly implement in terms of either equation (1) or (2). The only components required, other than basic circuit primitives, would be the ammeters at each port to sense the port current.

Since the goal of the macromodel is to reduce the linear circuit complexity and remove circuit stiffness, the port impedances (i.e. $z_{ii}(s)$ with $i = 1, N$) and the transimpedances (i.e. $z_{ij}(s)$ with $i, j = 1, N$ and $i \neq j$) are replaced by reduced order functions using AWE. For the model given by (2) it is obviously more advantageous to directly reduce the order of $f_{ij}(s)$. with $i, j = 1, N$ and $i \neq j$. For the remainder of this paper we will use a hat over a frequency domain function to denote a reduced order approximation of the basic variable (e.g. $\hat{V}(s)$ for $V(s)$).

III.1 Port impedance models

On chip RC-interconnect is often modeled by an RC tree or mesh, with no dc paths to ground. For such RC circuits, any node admittance can be described in terms of its poles and residues, or moments, as follows:

$$Y(s) = s \cdot \left(k_0 + \sum_{i=1}^{q} \frac{k_i}{s + p_i} \right) = \sum_{j=1} m_j \cdot s^j \tag{3}$$

Where the k_i's and p_i's are the residues and poles respectively, and m_i's are the moments.

The driving point immittance is modeled in terms of a reduced order admittance model:

$$\hat{Y}(s) = s \cdot \sum_{i=1}^{n} \frac{\hat{k}_i}{s + \hat{p}_i} = \sum_{i=1}^{n} \frac{s \cdot \hat{k}_i}{s + \hat{p}_i} \tag{4}$$

where all $\hat{k}_i$'s and $\hat{p}_i$'s are forced to be positive so that the approximation is stable and realizable [9]. From (4) we synthesize an equivalent circuit model for $\hat{Y}(s)$ [11], as shown in Fig. 3.

In Fig. 3, each term for the summation in (4) is implemented as

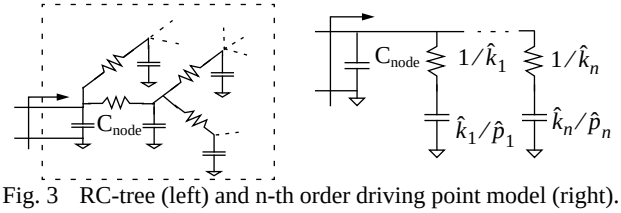

Fig. 3 RC-tree (left) and n-th order driving point model (right).

a single RC, series connection. For example, for the i-th element of the sum, the corresponding RC values are:

$$R_i = \frac{1}{\hat{k}_i} \text{ and } C_i = \frac{\hat{k}_i}{\hat{p}_i} \tag{5}$$

[1] SPECsim, AS/X and PowerPC are IBM Corporation trademarks.

III.2 Transmittance models

It is impossible to model transmittances in timing simulators without controlled source primitives. Due to their various waveshape assumptions, not all types of controlled sources are available in all timing simulators. For example, SPECS can handle only piecewise constant currents and piecewise linear voltages. As a consequence, only linear current controlled current sources and linear voltage controlled voltage sources are allowed. Also, while theoretically possible, MOSFET current sources as controlling sources and multiple controlling sources are not yet implemented.

There is no mention of any controlled source primitives in ELogic [2], but this does not mean that they are theoretically impossible. We would expect that linear voltage controlled voltage sources are the easiest to introduce in ELogic due to the modeling approach employed.

The type of controlling source chosen, i.e the "sensor," depends on the event type found in the simulator. In general, all timing simulators are able to compute both node voltage and cutset currents at any port, but usually only one is in the event table. Except for the few independent sources, for ELogic the node voltages and for SPECS the current sources modelling the dissipative elements generate the events. For SPECS, this restricts the type of controlled sources to current sources.

From (1) or (2) we know that the controlled sources type is not critical in choosing the type of port parameters. Therefore, we can avoid hybrid parameters and choose the description based on the available controlling sources. For this reason, we select *z*-parameters for SPECS and *y*-parameters for ELogic.

Using AWE it is possible to compute the moments of the short-circuit current or open-circuit voltage at the ports when the circuit is driven by a current or voltage source at one port, and all other ports are short- or open-circuited. For example, to obtain f_{ij} from (2), we open-circuit all ports except *i* and *j*, and measure the short-circuit current response at node *i* due to a current source applied at node *j*. These transmittance moments are then used to generate reduced order transmittance functions.

From *2n* transmittance moments is possible to compute an *n*-th order pole-residue AWE model of the form:

$$\hat{H}_{ij}(s) = \sum_{l=1}^{n} \frac{\hat{k}_{ij(l)}}{s + \hat{p}_{ij(l)}} \qquad (6)$$

There are at least two ways of implementing the reduced order transmittance functions: a) linear controlled sources and physical circuits to realize the poles, or b) special purpose interconnect macromodels to optimize the simulator performance [11]. For physical circuit representations, the suggested model for ELogic is given in Fig. 4a, while that for SPECS is shown in Fig. 4b. Each pole RC component has only one constraint: the RC product is equal to the reciprocal pole value. For ELogic we are free to arbitrarily select the values for R and C, however, for SPECS the problem is more complicated.

In SPECS, the resistor model resolution is given by the voltage step in the current-voltage table (i.e. the largest voltage interval for which the resistor model current is constant). For a given resolution, v_ε, two unwanted cases can occur: the voltage drop across the resistor is much greater than v_ε, or much smaller than v_ε. In the first case, too many events are generated and the simulation efficiency is greatly affected. For the actual resistor in a circuit with only grounded capacitors and no inductors, the voltage swing is bounded by V_{DD}. But this is not the case for the pole circuits shown in Fig. 4b. Unrealistic voltages can occur across these fabricated entities. For the case when the voltage drop is much smaller than v_ε, no event is generated and the resistor information is lost. Both issues are critical for these pole circuits, so we propose the following solution.

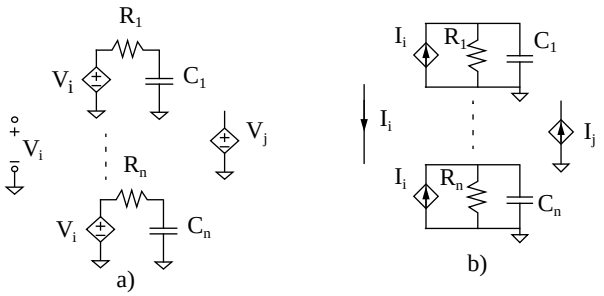

Fig. 4 Representation of (6) with controlled sources and physical elements: a) using voltage controlled voltage sources; b) using current controlled current sources.

We observe that, for RC networks driven at only one port, the driver current that charges the total network capacitance (C_{tot}) to V_{DD} is the same total current into the pole circuits. Consequently, it can be shown from a charge conservation perspective that the voltage on any pole circuit is less than or equal to V_{DD}. So, by choosing all C_l's in Fig. 4b equal to C_{tot} we bound the number of events for R_l's, for a given v_ε. Experimentally we determined that this value also handles the lowest voltage drop problem.

Although it is possible to implement the proposed N-port macromodel in timing simulators with existing primitives (i.e. controlled sources, R's and C's), it can be implemented with the utmost efficiency in terms of a dedicated macromodel [11].

IV. RESULTS

SPECS has the ability to model MOS transistors and resistors with variable resolution. In our experiments we used MOS table models having a resolution of 50mV, and resistor table models with resolutions of 2mV, 10mV and 50mV. In the following tables we use the name SPECS*x*mV for SPECS using 50mV table models for MOS transistors and *x*mV table models for resistors.

We tested the macromodel on thousands of nets from a PowerPC chip. A digital circuit with 13,407 linear components is used to demonstrate the efficiency of the SPECS macromodels for interconnects with one driving port (the usual case on-chip). This circuit is driven by a chain of three inverters. We used a 2^{nd} order driving point model and a two-pole transmittance model as required by accuracy considerations. Fig. 5 shows SPECS results as compared with AS/X when using macromodels for both. The flattened circuit could not be simulated in SPECS but the AS/X analysis of the flattened circuit agreed with the macromodel results.

Table 1 displays the simulation times. As for all other circuits we simulated, two interesting observations should be made: a) SPECS is unable to simulate the full circuit and b) the runtime difference between SPECS10mV and SPECS50mV is not significant. Experimentally, we determined that the accuracy of SPECS10mV is generally acceptable, better resistor model resolution is not required.

The SPECS speed-up shown in Table 1 is typical for small circuits. To verify this we compared SPECS and AS/X for the same chain of inverters driving a single capacitive load. The confirming results shown in Table 2 confirm this speed-up.

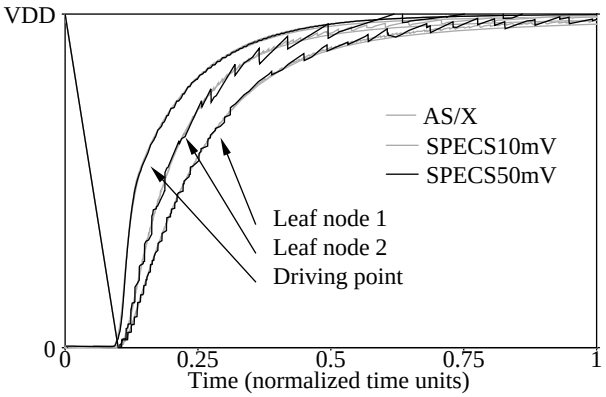

Fig. 5 AS/X vs. SPECS for a chain of three inverters driving a 13,407 linear components network.

Table 1: Simulation time for a 13,407 components network with one driving port and two observation ports

	time (s)	# of events	speed-up
AS/X full network	168	-	-
AS/X macromodel	10.1	-	1x
SPECS50mV macromodel	0.99	3,989	10.2x
SPECS10mV macromodel	1.02	6,314	9.9x
SPECS2mV macromodel	1.5	16,880	6.73x
SPECS flattened circuit (any table size)	N/A	N/A	N/A

Table 2: Simulation time for capacitive load.

	time (s)	# of events	speed-up
AS/X	9.1	-	1x
SPECS10mV	0.84	1,026	10.8x

We next consider another clock net from a PowerPC circuit which contained two driving ports. The runtime results are given in Table 3, the waveforms are shown in Fig. 6.

Table 3: Simulation time for a circuit with two driving ports

	time (s)	# of events	speed-up
AS/X	11.3	-	1x
SPECS10mV	1.29	8,924	8.76x

It is important to note that once the circuit stiffness is removed, the number of resistor events in SPECS, namely N_{evR}, becomes proportional with n_R, the number of resistors. If n_a and n_t represent the admittance model order and transmittance order respectively, then we have:

$$n_R = N \cdot n_a + k \cdot N \cdot n_t \tag{7}$$

where k is the number of driving ports and N is the total number of ports, thereby making N_{evR} linear in terms of the number of ports, [11]. If k is close to N, however:

$$N_{evR} = O\left(N^2\right) \tag{8}$$

Moreover, the N-port macromodel forms a dense NxN matrix in a circuit simulator. To solve this dense matrix in any SPICE- or ASTAP-like circuit simulator will require $O(N^3)$ operations.

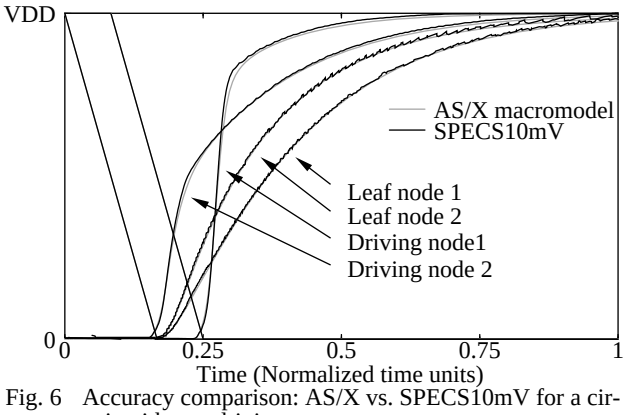

Fig. 6 Accuracy comparison: AS/X vs. SPECS10mV for a circuit with two driving ports.

V. CONCLUSIONS

The main conclusion of our work is that the interconnect macromodels for timing simulators, particularly for SPECS, are feasible, and more importantly, extremely effective. Moreover, large macromodels in SPICE are inefficient since the Newton-Raphson linearized models at the ports require that we invert the large, dense, *Y* matrix at every Newton-Raphson iteration. This can become more costly than simulating the flattened circuit if there are a large number of ports (like for a clock tree). In SPECS, the piecewise constant device models allow us to easily superpose the various current responses.

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