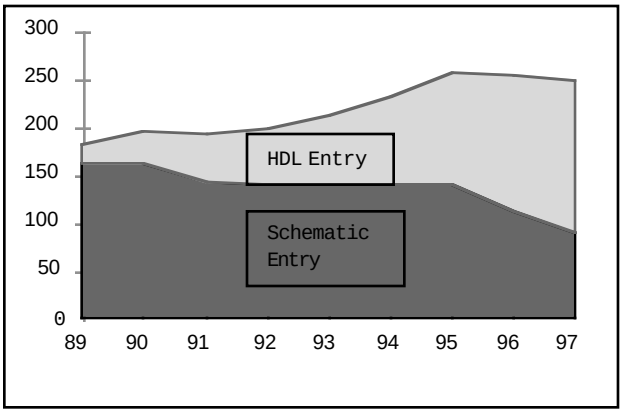
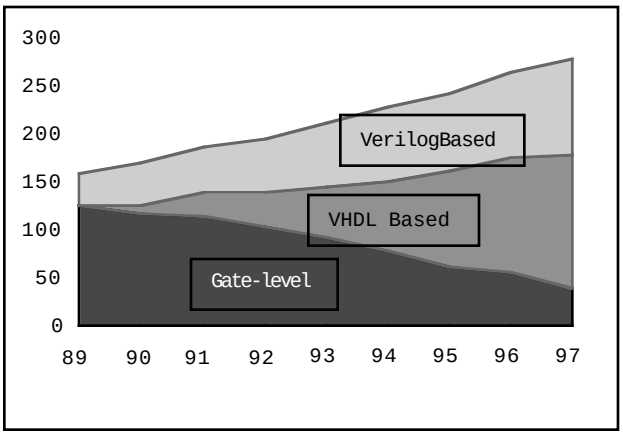
RTL Emulation: The Next Leap In System Verification
Authors: Sanjay Sawant and Paul Giordano

The worldwide electronics market is booming, fueled by the customers' insatiable appetite for low-cost computers, connectivity and appliances packed with high-technology features. While the sheer number of new design starts may not be noteworthy, the development of new chips and systems that are becoming more complex at a phenomenal rate.

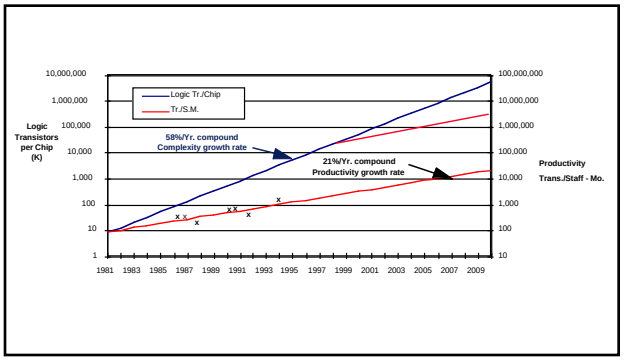
The effect of increase in design complexity is dual fold. First, designers are quickly migrating to higher levels of abstraction. Production use of text-based methodology has enabled designers to capture designs of hundreds of thousands of gates using graphic ESDA tools.





Source: Data Quest (Verilog/VHDL Market SpecialReport)

Second, is the change in manufacturing process. Today, designers are using 0.35 micron or even 0.25 micron technology. Submicron manufacturing capabilities enable millions of gates on a single chip. Sematech predicts that 0.25 micron technology will be ubiquitous by 1998 and the average chip complexity will be 20 million transistors. With most ASIC fabs running 0.5 micron processes reliably, and several delivering or scheduling a move to 0.25 micron soon, manufacturing capabilities are quickly outgrowing the capacity of current design tools.



The obstacles in developing new generation of electronics revolve around three key questions:

1. Can we design such complex chips and systems?
2. Can our factories fabricate these designs?
3. Can we verify the accuracy of these complex designs?

The advances in high level design brought about by languages such as Verilog and VHDL coupled with logic synthesis technologies has largely addressed the first question.

To answer the second question, semiconductor fabrications can now put millions of logic gates on a single chip using deep sub-micron technology. This rapid increase in the complexity of chips and systems has outstripped traditional verification techniques. This is further complicated when a chip or an ASIC is plugged into the final system. This is because of The famous 90/50 rule. Accordingly 90% of ASICs will work first time when tested stand-alone. However, only 50 % will work right when brought into the final system. A typical system level sign-off requires billions of clock cycles. When using traditional verification techniques, based upon software simulation, it will be several months, maybe even years before you can obtain a system sign-off in applications. Such as Real Time Video, ATM, PCI Protocols and DSP applications. In a typical MPEG video compression design it is not uncommon to visually verify 5 seconds of real time decoded video (about 150 frames). Using RTL simulation tools running at 46 HZ, it would take four hours per frame: a total of 200 hours (25 twenty-four hour days) to accomplish the desired system verification goal. In the development of an Infrared Search and Track (IRST) processing system (an early Rapid Prototyping of Application Specific Signal Processors — RASSP), simulation run times were so slow that only those activities near the beginning of the hardware initialization cycle (the first 150 milliseconds) were explored. As a result, system verification has become the main bottleneck in the development of complex "system on silicon" particularly in light of increasing time to market pressures.

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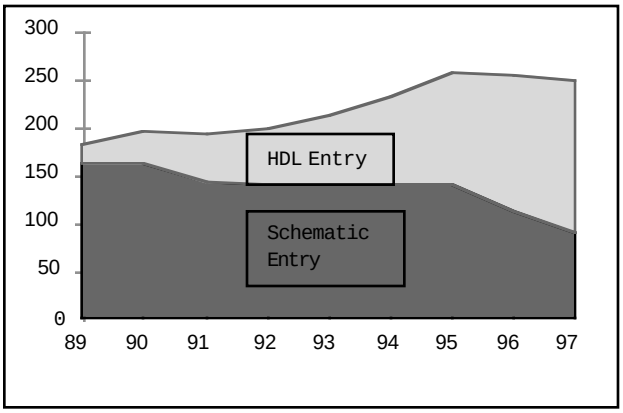

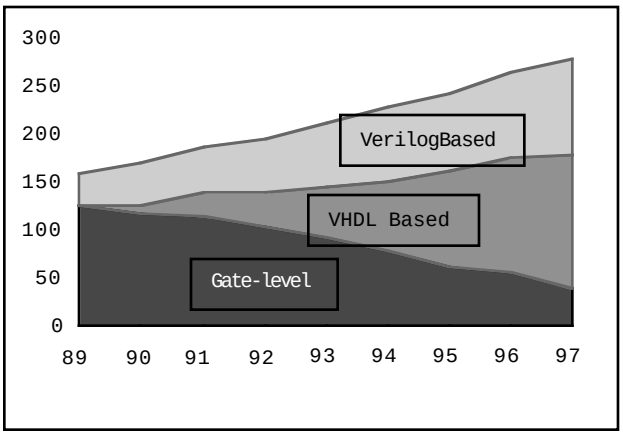

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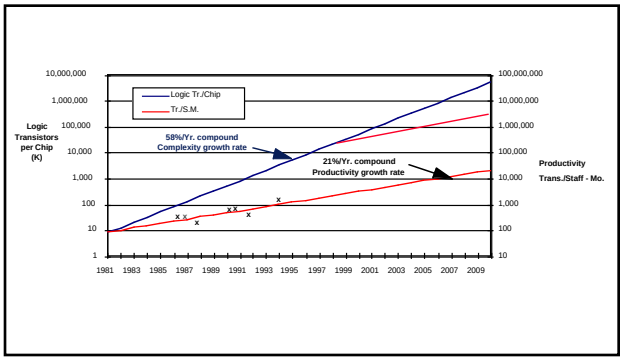

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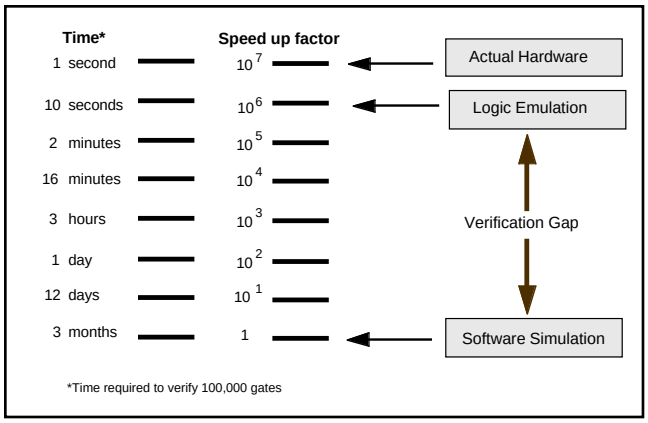
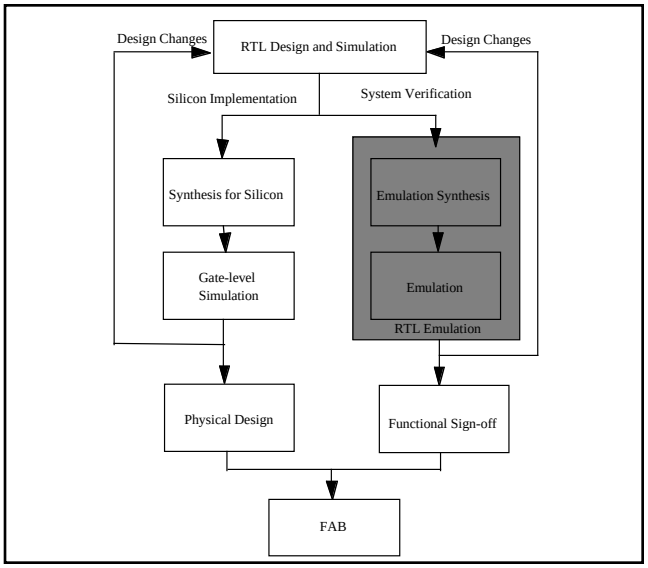


Considering the complexity of projects, today's designs require a different verification technique. One that is independent of design complexity. That technique is Emulation. Emulation is a technology that enable designers to imitate the logic of their designs in the form of a reprogrammable devices or processors. Once programmed, an emulator represents a virtual silicon that can be directly interfaced with the target system. The beauty of emulation is its ability to verify designs at megahertz speeds and have the ability to go in-circuit.

Today hardware implementation has been greatly automated by logic synthesis. Considering today's design complexity it is virtually impossible to combine implementation path with the verification path. Designers need to validate their RTL in a context of the entire system prior to silicon synthesis. Most of the commercially available synthesis tools spend time optimizing designs for silicon. However, a synthesis tool required for system validation has different requirements. First, 100% source level visibility between RTL and gate-level domain with the exception of the primary I/Os between hierarchical modules, current synthesis tools are unable to preserve net names from the gate-level back to RTL. As a result, designers need to debug their designs at user unfriendly gate-level description. Performance is also an important factor. Today significant time is spent on manually partitioning the design into small blocks of manageable size to achieve reasonable performance from the synthesis engine. An ultimate objective of the system verification engineer is to validate RTL in the context of the system as early as possible. Therefore superfast performance with reasonable optimization is also important.

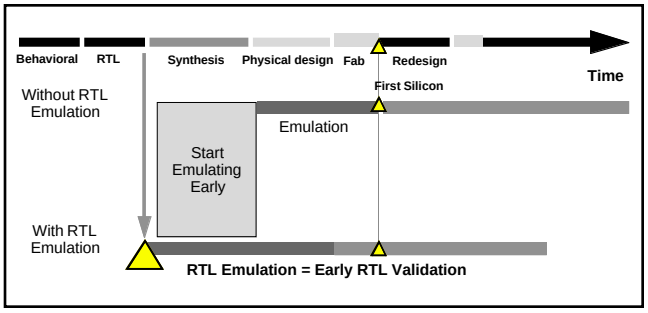
Recently a technology has emerged that combines RTL synthesis with emulation. RTL Emulation is directed at solving the debugging limitations inherent in the traditional system verification tools and moving emulation to a higher-level of abstraction. This technology provides 100% source-level visibility that enables debugging at RTL level. Designers can directly correlate bugs found during emulation to RTL description. With RTL emulation, emulation becomes an evolutionary step after block-level simulation. RTL emulation enables users to deal with increased design complexity by separating design implementation from design verification. A user can validate RTL in context of entire system much earlier in the design cycle. One can visualize the effect of plugging in RTL inside the final system.



The core of RTL Emulation is a synthesis engine that enables users to map their mixed-level designs to emulation database. The technology provides mapping that is optimal for Quickturn's hardware box. It maps memory description from RT level down to hard macros. Control logic and data-path optimization are handled by different algorithms. Users can supply constraints to control the emulation process, such as clock sources, internal probes, etc., at RTL level using synthesis directives. An incremental synthesis process enables fast iterative changes to a design. An incremental synthesis is closely coupled with source level EOO. This enables designers to reflect their RTL changes to an emulation model.

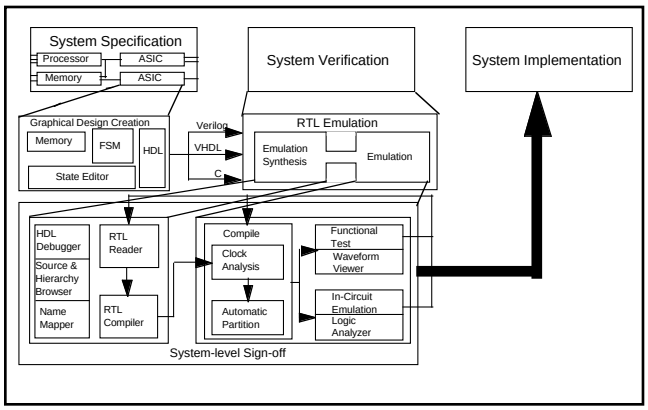
The benefits of RTL Emulation include:

- Early RTL validation in context of an entire system.
- Assurance that the RTL model is really golden before the synthesis phase begins.
- Support for multi-million gate design.



RTL Emulation technology is architected to easily handle large designs. A graphical hierarchy browser and drag & drop source browser facilitate error tracing. Users can directly select RTL nets for probing purposes during emulation. The logic browser enables designers to select a net from the waveform viewer to view its drivers and their contributing values.

After RTL mapping, an emulation database is generated and is passed on to the core emulation software. The core emulation software includes a partitioner, compiler, and a suite of diagnostics. The partitioner divides emulation databases into smaller blocks that can be targeted for individual boards within an emulator and then onto individual FPGAs on the board. Once partitioned, the compiler performs placement and routing between FPGAs and generates a bit pattern. This is used to program an emulator. Once an emulation model is generated, it can be validated by using the same vector set for simulation. Designers can start debugging their designs by directly interfacing an emulator with their target system. The majority of emulators come equipped with a logic analyzer, and a waveform viewer. Waveform display is tightly coupled with the source browser. This enables designers to locate the culprit RTL code. Designers can also perform extensive debugging using breakpoints, single-stepping, etc.



RTL Emulation offers faster mapping and megahertz performance, designers can have multiple spins of their designs while dramatically shortening their silicon development schedule. With simplicity, performance, and an intelligent debugging capability offered early in the design cycle, RTL Emulation can ensure full system-level verification, high product quality and early market entry.