Short Paper Session 4 : Power Optimization and Charge Recovery Techniques

S4.1 Re-Encoding for Low Power State Assignment of FSMs
V. Veeramachaneni, A. Tyagi, and S. Rajgopal, Iowa State Univ., Ames, IA

S4.2 Optimization of Power Dissipation and Skew Sensitivity in Clock Buffer Synthesis
J.W. Chung, D-Y. Kao, C-K. Cheng, and T-T. Lin, Univ. of California, San Diego, CA

S4.3 Charge Recovery on a Databus
K-Y. Khoo, and A.N. Wilson, Jr., UCLA, Los Angeles, CA

S4.4 2nd Order Adiabatic Computation with 2N-2P and 2N-2N2P Logic Circuits
A. Kramer, J.S. Denker, B. Flower, and J. Mulrony, AT&T Bell Lab., Holmdel, NJ