Short Paper Session 2: Architectural Issues

S2.1 Cache Design Trade-Offs for Power and Performance Optimization: A Case Study
C-L. Su, and A.M. Despain, USC, Los Angeles

S2.2 Simultaneous Scheduling and Binding for Power Minimization During Microarchitecture Synthesis
A. Dasgupta, and R. Karri, Univ. of Massachusetts, Amherst, MA

S2.3 Overview of the Power Minimization Techniques Employed in the IBM PowerPC 4xx Embedded Controllers
A. Correale, Jr., IBM, RTP, NC