Regular Session 6 : Physical Design for Low Power

Session Chair: Jason Cong, UCLA

6.1 Power and Area Optimization by Reorganizing CMOS Complex-Gate Circuits
M. Tachibana, S. Kurosawa, R. Nojima, N. Kojima, M. Yamada, T. Mitsuhashi, and N. Goto, Toshiba, Kawasaki, Japan

6.2 Transistor Reordering for Low Power CMOS Gates Using and SP-BDD Representation
A.L. Glebov, D. Blaauw, and L.G. Jones, Motorola, Austin, TX

6.3 Transistor Sizing for Minimizing Power Consumption of CMOS Circuits Under Delay Constraint
M. Borah, R. Owens, and M-J. Irwin, Pennsylvania State Univ., University Park, PA