Regular Session 2: Software and System Level Issues

Session Chair: Mani Srivastava, AT&T

2.1 Energy Optimization of Multi-Level Processor Cache Architectures
U. Ko, A. K. Nanda, and P.T. Balsara, TI, Dallas, TX

2.2 Transforming Set Data Types to Power Optimal Data Structures
S. Wuytack, F. Catthoor, and H. De Man, IMEC, Leuven, Belgium

2.3 Reducing the Frequency of Tag Compares for Low-Power I-Cache Design
R. Panwar, and D. Rennels, UCLA, Los Angeles, CA