Session 7C
Gate Sizing

Moderators: Hidetoshi Onodera
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7C.1 A Delay Model for Logic Synthesis of Continuously-Sized Networks
J. Grodstein, E. Lehman, H. Harkness, B. Grundmann, and Y. Watanabe

7C.2 Power vs. Delay in Gate Sizing: Conflicting Objectives?
S.S. Sapatnekar and W. Chuang

7C.3 Speeding Up Pipelined Circuits through a Combination of Gate Sizing and Clock Skew Optimization
H. Sathyamurthy, S.S. Sapatnekar, and J.P. Fishburn