Session 7A
Power and Delay Optimization in Synthesis

Moderators: Sujit Dey
Michel Berkelaar

7A.1 An Iterative Gate Sizing Approach with Accurate Delay Evaluation
G. Chen, H. Onodera, and K. Tamaru

7A.2 Boolean Techniques for Low Power Driven Re-Synthesis
R.I. Bahar and F. Somenzi

7A.3 Two-Level Logic Minimization for Low Power
S. Iman and M. Pedram