Session 6A
FPGA Synthesis

Moderators: Bob Francis
Albert Wang

6A.1 Technology Mapping for Field-Programmable Gate Arrays Using Integer Programming
A. Chowdhary and J.P. Hayes

6A.2 Logic Synthesis for Look-Up Table Based FPGAs Using Functional Decomposition and Support Minimization
H. Sawada, T. Suyama, and A. Nagoya

6A.3 Compatible Class Encoding in Roth-Karp Decomposition for Two-Output LUT Architecture
J.-D. Huang, J.-Y. Jou, and W.-Z. Shen