Session 5D
FPGA Routing

Moderators: Dwight Hill
Y. Kajitani

5D.1 An Empirical Model for Accurate Estimation of Routing Delay in FPGAs
T. Karnick and S.M. Kang

5D.2 Performance-Driven Simultaneous Place and Route for Island-Style FPGAs
S.K. Nag and R.A. Rutenbar

5D.3 Board-Level Multi-Terminal Net Routing for FPGA-Based Logic Emulation
W.-K. Mak and D.F. Wong