Session 5A
Advances in Logic Synthesis

Moderators: Robert K. Brayton
Gary Hachtel

5A.1 Efficient Orthonormality Testing for Synthesis with Pass-Transistor Selectors
M. Berkelaar and L.P.P.P van Ginneken

5A.2 Logic Decomposition during Technology Mapping
E. Lehman, Y. Watanabe, J. Grodstein, and H. Harkness

5A.3 Efficient Use of Large Don’t Cares in High-Level and Logic Synthesis
R.A. Bergamaschi, D. Brand, L. Stok, M. Berkelaar, and S. Prakash