Session 2A
DCs and DDs in Logic Synthesis

Moderators: Michel Berkelaar
            Sujit Dey

2A.1 Who Are the Variables in Your Neighborhood
    S. Panda and F. Somenzi

2A.2 Efficient Construction of Binary Moment
    Diagrams for Verifying Arithmetic Circuits
    K. Hamaguchi, A. Morita, and S. Yajima

2A.3 Be Careful with Don’t Cares
    D. Brand, R.A. Bergamaschi, and L. Stok