Session 1A
Formal Verification

Moderators: Ellen M. Sentovich
David E. Long

1A.1 Efficient Validity Checking for Processor Verification
R.B. Jones, D.L. Dill, and J.R. Burch

1A.2 The Formal Verification of a Pipelined Double-Precision IEEE Floating-Point Multiplier
M.D. Aagaard and C.-J.H. Seger

1A.3 Extracting RTL Models from Transistor Netlists
K.J. Singh and P.A. Subrahmanyam