1995
IEEE/ACM International Conference on Computer-Aided Design

November 5–9, 1994 San Jose, California

Digest of Technical Papers

IEEE Computer Society Press
Los Alamitos, California

Washington • Brussels • Tokyo

IEEE Computer Society Press
10662 Los Vaqueros Circle
P.O. Box 3014
Los Alamitos, CA 90720-1264

IEEE Computer Society Press Order Number PR07213
IEEE Order Plan Catalog Number 95CB35859
Library of Congress Number 86-646631
ISBN 0-8186-7213-7
Microfiche ISBN 0-8186-7214-5
IEEE Order Plan ISBN 0-8186-7215-3
ISSN 1063-6757

Additional copies may be ordered from:

IEEE Computer Society Press
Customer Service Center
10662 Los Vaqueros Circle
P.O. Box 3014
Los Alamitos, CA 90720-1264
Tel: +1-714-821-8380
Fax: +1-714-821-4641
Email: cs.books@computer.org

IEEE Service Center
445 Hoes Lane
P.O. Box 1331
Piscataway, NJ 08855-1331
Tel: +1-908-981-1393
Fax: +1-908-981-9667
misc.custserv@computer.org

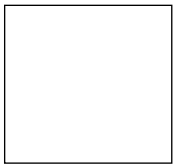
IEEE Computer Society
13, Avenue de l'Aquilon
B-1200 Brussels
BELGIUM
Tel: +32-2-770-2198
Fax: +32-2-770-8505
euro.ofc@computr.org

IEEE Computer Society
Ooshima Building
2-19-1 Minami-Aoyama
Minato-ku, Tokyo 107
JAPAN
Tel: +81-3-3408-3118
Fax: +81-3-3408-3553
tokyo.ofc@computer.org

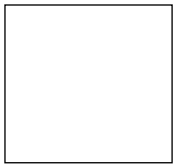
Editorial production by Penny Storms
Cover by MP Associates
Printed in the United States of America by KNI, Inc.

The Institute of Electrical and Electronics Engineers, Inc.

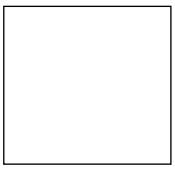
CONFERENCE COMMITTEE



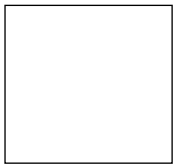
CONFERENCE CHAIR
Richard Rudell
Synopsys, Inc.
700 E. Middlefield Rd.
Mountain View, CA 94043-4033
(415) 694-4337
rudell@synopsys.com



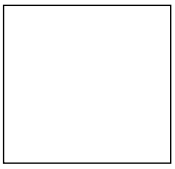
PROGRAM CHAIR
Rob A. Rutenbar
Carnegie Mellon Univ.
Dept. of ECE
5000 Forbes Ave.
Pittsburgh, PA 15213
(412) 268-3334
rutenbar@ece.cmu.edu



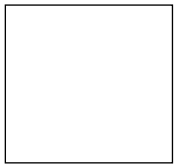
AUDIO-VISUAL CHAIR
David Ku
Escalade Corp.
1210 E. Arques Ave.
Sunnyvale, CA 94086
(408) 481-1317
ku@escalade.com



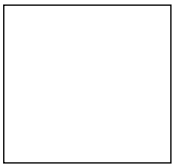
PUBLICATIONS CHAIR
Ralph H.J.M. Otten
Delft Univ. of Technology
Lab. for Circuits & Sys., Dept. EE
Mekelweg 4, 2628 CD Delft
The Netherlands
(31) 15-781600
otten@muresh.et.tudelft.nl



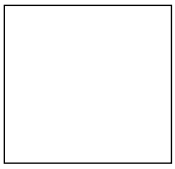
ASIAN REPRESENTATIVE
Youn-Long Lin
Tsing Hua Univ.
Dept. of CS
Hsin-Chu, Taiwan 30043 ROC
(886) 35-731072
ylin@cs.nthu.edu.tw



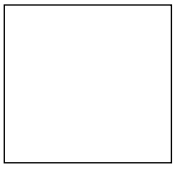
PAST CHAIR
Jochen A.G. Jess
Eindhoven Univ. of Technology
Design Auto. Sec., Dept. EE
E-hoog, Den Dolech 2, 5612 AZ Eindhoven
The Netherlands
(31) 40-473353
jess@es.ele.tue.nl



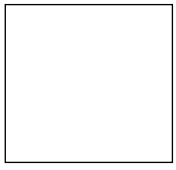
EUROPEAN REPRESENTATIVE
Kurt J. Antreich
Technical Univ. of Munich
Dept. of ECE, Rm. 3909
Arcisstr. 21, D-80333
Munich, Germany
(49) 89-2105-3677
antreich@e-technik.tu-muenchen.de



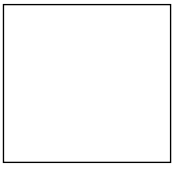
PUBLICITY CHAIR
Mary Bailey
Univ. of Arizona
Gould-Simpson Bldg., #721
Dept. of CS
Tucson, AZ 85721
(602) 621-4526
mlb@cholla.cs.arizona.edu



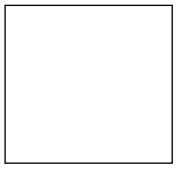
SIGDA REPRESENTATIVE
Robert A. Walker
Rensselear Polytechnic Inst.
Dept. of CS
Troy, NY 12180-3590
(518) 276-8275
walker@cs.rpi.edu



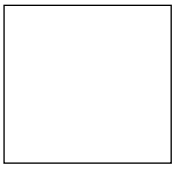
TUTORIAL CHAIR
William H. Joyner, Jr.
IBM Corp.
TJ Watson Research Ctr.
PO Box 218
Yorktown Heights, NY 10589
(914) 945-1057
joyner@watson.ibm.com



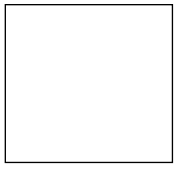
IEEE CS/DATC REPRESENTATIVE
Charles W. Rosenthal
CWR-Engineering Consultants
3080 SW Fairmont Blvd.
Portland, OR 97201-1439
(503) 245-8398
charlier@cse.ogi.edu



PANEL SESSION CHAIR
Daniel D. Gajski
Univ. of California
Dept. of CS
Irvine, CA 92717-3425
(714) 856-8095
gajski@ics.uci.edu



CONFERENCE MANAGER
Kevin Lepine
MP Associates, Inc.
5305 Spine Rd., Ste. A
Boulder, CO 80301
(303) 530-4562
kevin@dac.com



LOCAL ARRANGEMENTS
FINANCE CHAIR
Robert C. Aitken
Hewlett-Packard Co.
Design Tech. Ctr., M/S- 6UK
1501 Page Mill Rd.
Palo Alto, CA 94303-0889
(415) 857-2146
aitken@dtc.hp.com

FOREWORD

On behalf of the ICCAD-95 Executive and Technical Program Committees, we would like to welcome you to the 13th installment of the International Conference on Computer-Aided Design. We return this year to the San Jose Red Lion Hotel with its convenient conference room facilities and cozy atmosphere. We have worked hard to hold down the cost of attending ICCAD-95 by maintaining a low nightly rate for hotel rooms.

The Technical Program for ICCAD-95 was put together under the direction of Rob A. Rutenbar. The Technical Program Committee was organized as 13 subcommittees each with a focus in a specific technical area. Each subcommittee had up to seven experts in the field evaluating about 30 technical papers of which less than one third could fit into the technical program. The subcommittee members represented a diverse range of opinions and included members from industry and academia, and included significant international representation. Each volunteer on the committee devoted many hours reviewing each paper and then attended the full day committee meeting to present and defend their reviews and to assist in the difficult process of choosing a small subset of the papers for ICCAD-95. Overall, only 108 of the 350 papers submitted to ICCAD-95 were accepted to appear at the conference.

Within the technical track, we have included four 90 minute tutorials. Research experts in their respective fields will introduce the basic concepts in technical areas which are at the forefront of CAD research today: Boolean manipulation algorithms that make formal verification practical; modern analysis techniques necessary for interconnect-dominated designs; new power estimation techniques being developed for complex ICs; and, the embedded system design challenges posed by multimedia ICs.

We have also included two panels in the technical program. Continuing on a theme from the Design Automation Conference where several prominent EDA Chief Executive Officers (CEO's) were asked to talk about their business, we have asked several prominent EDA Chief Technology Officers (CTO's) and Chief Scientists to talk about their technology at a panel on Monday evening titled "Chief Technologists Tell All: What's Hot? What's Not? What's Next?". An open question in the EDA industry is figuring out how the availability of 20M+ gate designs will change the tools and design methodologies of the systems designer. One dimension of the next generation system design methodology will be explored in our Wednesday afternoon panel titled "Are Parameterized Cores a Serious Business?".

Complementing the technical program is the 1995 Tutorial Program organized by William Joyner, Jr. The four full-day tutorials on Thursday, November 9 offer in-depth information on established areas of CAD where outstanding speakers and educators outline their respective technical fields. This year the tutorial topics include: Practical Aspects of Formal Hardware Verification, Hardware/Software Codesign of Embedded Systems, Optimization Techniques for Low Power VLSI Circuits, and The Systematic Design of Asynchronous Circuits. These tutorials have always been an important part of ICCAD and generate positive feedback from the tutorial attendees.

Many things have changed in our industry since the first ICCAD was held in Santa Clara in 1983. Increasing design complexity has spawned a seemingly unlimited number of technical challenges which has also led to a high degree of specialization within the EDA industry. It is our sincere hope that ICCAD-95 fills the role of bringing together specialists in the many technical areas within CAD with the goal of addressing the broad range of IC and System design problems.

Richard Rudell
Conference Chair

Rob A. Rutenbar
Technical Program Chair

ICCAD-95 TECHNICAL PROGRAM COMMITTEE

Robert C. Aitken
Hewlett-Packard Co.
Palo Alto, CA

Kurt J. Antreich
Technical Univ. of Munich
Munich, Germany

Mary Bailey
Univ. of Arizona
Tucson, AZ

Jacques Benkoski
EurEPIC
Gieres, France

Reinaldo Bergamaschi
IBM Corp.
Yorktown Heights, NY

Michel Berkelaar
Eindhoven Univ. of Tech.
Eindhoven, The Netherlands

Gaetano Borriello
Univ. of Washington
Seattle, WA

Jay Brockman
Univ. of Notre Dame
Notre Dame, IN

Philip C.H. Chan
The Hong Kong Univ. of Sci./Tech.
Kowloon, Hong Kong

Kwang-Ting Cheng
Univ. of California
Santa Barbara, CA

Jue-Hsien Chern
Technology Modeling Assoc., Inc.
Palo Alto, CA

Jason Cong
Univ. of California
Los Angeles, CA

Bernard Conq
CNET-Grenoble
Meylan, France

Olivier Coudert
Synopsys, Inc.
Mountain View, CA

Bernard Courtois
TIMA
Grenoble, France

Srinivas Devadas
Massachusetts Inst. of Tech.
Cambridge, MA

Sujit Dey
C&C Res. Labs., NEC USA, Inc.
Princeton, NJ

Nikil Dutt
Univ. of California
Irvine, CA

Peter Feldmann
AT&T Bell Labs.
Murray Hill, NJ

Bob Francis
Xilinx Toronto Dev. Ctr.
Toronto, Ontario, Canada

Georges Gielen
Katholieke Univ.
Heverlee, Belgium

Michaela Guiney
Hewlett-Packard Co.
Palo Alto, CA

Gary Hachtel
Univ. of Colorado
Boulder, CO

Michel Heydemann
Consultant
Palaiseau, France

Dwight Hill
Synopsys, Inc.
Mountain View, CA

Tamotsu Hiwatashi
Toshiba Corp.
Kawasaki, Japan

Masaharu Imai
Toyohashi Univ. of Tech.
Toyohashi, Japan

Margarida F. Jacome
Univ. of Texas
Austin, TX

Rajeev Jayaraman
Xilinx, Inc.
San Jose, CA

Frank M. Johannes
Technical Univ. of Munich
Munich, Germany

Andrew B. Kahng
Univ. of California
Los Angeles, CA

Y. Kajitani
Tokyo Institute of Tech.
Tokyo, Japan

Takashi Kambe
Sharp Co.
Nara, Japan

ICCAD-95 TECHNICAL PROGRAM COMMITTEE

David Ku
Escalade Corp.
Sunnyvale, CA

Sy-Yen Kuo
National Taiwan Univ.
Taipei, Taiwan, ROC

Luciano Lavagno
Politecnico di Torino
Torino, Italy

David Lewis
Univ. of Toronto
Toronto, Ontario, Canada

Chen-Shang Lin
National Taiwan Univ.
Taipei, Taiwan, ROC

Youn-Long Lin
Tsing Hua Univ.
Hsin-Chu, Taiwan, ROC

David Ling
IBM Corp.
Yorktown Heights, NY

David Long
AT&T Bell Labs.
Murray Hill, NJ

Fadi Maamari
AT&T Bell Labs.
Princeton, NJ

Don MacMillen
Synopsys, Inc.
Mountain View, CA

Sharad Malik
Princeton Univ.
Princeton, NJ

Wojciech Maly
Carnegie Mellon Univ.
Pittsburgh, PA

Margaret Marek-Sadowska
Univ. of California
Santa Barbara, CA

Peter Maurer
Univ. of South Florida
Tampa, FL

Peter Maxwell
Hewlett-Packard Co.
Palo Alto, CA

Patrick McGeer
Cadence Berkeley Labs.
Berkeley, CA

Farid Najm
Univ. of Illinois
Urbana, IL

Yukihiro Nakamura
NTT Knowledge Systems Lab.
Yokosuka-Shi, Japan

Sani Nassif
AT&T Bell Labs.
Allentown, PA

Hidetoshi Onodera
Kyoto Univ.
Kyoto, Japan

Ralph Otten
Delft Univ. of Tech.
Delft, The Netherlands

Lawrence T. Pileggi
Univ. of Texas
Austin, TX

Irith Pomeranz
Univ. of Iowa
Iowa City, IA

Miodrag Potkonjak
C&C Res. Labs., NEC USA, Inc.
Princeton, NJ

Dhiraj K. Pradhan
Texas A&M Univ.
College Station, TX

Janusz Rajski
Mentor Graphics Corp.
Wilsonville, OR

June-Kyung Rho
LG Info. & Communication Ltd.
Kyongki-Do, Korea

Wolfgang Rosenstiel
Univ. Tuebingen
Tuebingen, Germany

Takayasu Sakurai
Toshiba Corp.
Kawasaki, Japan

Majid Sarrafzadeh
Northwestern Univ.
Evanston, IL

Ellen M. Sentovich
Ecole des Mines de Paris
Sophia-Antipolis, France

Fabio Somenzi
Univ. of Colorado
Boulder, CO

Tom Szymanski
AT&T Bell Labs.
Murray Hill, NJ

ICCAD-95 TECHNICAL PROGRAM COMMITTEE

Toshio Takamine
Hitachi, Ltd.
Kanagawa, Japan

Theodor Vierhaus
GMD
Sankt Augustin, Germany

Wayne Wolf
Princeton Univ.
Princeton, NJ

Don Thomas
Carnegie Mellon Univ.
Pittsburgh, PA

Kees A. Vissers
Philips Research Labs.
Eindhoven, The Netherlands

Andrew T. Yang
Univ. of Washington
Seattle, WA

Steve Tjiang
Synopsys, Inc.
Mountain View, CA

Kazutoshi Wakabayashi
Stanford Univ.
Stanford, CA

Hiroto Yasuura
Kyushu Univ.
Fukuoka, Japan

Louise Trevillyan
IBM Corp.
Yorktown Heights, NY

Albert Wang
Synopsys, Inc.
Mountain View, CA

Gary Yeap
Motorola, Inc.
Tempe, AZ

Ren-Song Tsay
ArcSys, Inc.
Sunnyvale, CA

Jacob White
Massachusetts Inst. of Tech.
Cambridge, MA

Yervant Zorian
AT&T Bell Labs.
Princeton, NJ

PANEL

CHIEF TECHNOLOGISTS TELL ALL: WHAT'S HOT? WHAT'S NOT? WHAT'S NEXT?

Moderator: *Rob A. Rutenbar* - Carnegie Mellon Univ., Pittsburgh, PA

When it comes right down to it, there are only two things that matter in EDA: money and ideas. Our sister conference--the Design Automation Conference--has a yearly panel of CEOs from EDA vendors in which everybody talks about money. Yet ideas remain the real fuel for this industry. And since ICCAD is a conference about ideas, it's our job to ask the tough questions: What will be the killer applications available from vendors in the coming decade? What are the nasty problems that we really need solved? What are the fashionable dead-ends that make nice papers but just aren't going to make it in the real world? In a shifting business and university climate, where will the new ideas come from? And how will they get filtered into final products: how does a neat idea become valuable intellectual property?

For answers, ICCAD goes directly to the source: Chief Technologists, Chief Scientists, and R&D Directors at a cross-section of EDA's most visible companies. Representing both software and silicon producers, and with backgrounds ranging from academic to entrepreneur, our panelists are uniquely positioned to address these issues. Join us as a set of outspoken technologists offers a glimpse of their visions for next-generation tools and technologies, and their answers to these and other questions from the moderator and audience.

Panel Members:

Carlos Dangelo - V.P. of Software R&D, LSI Logic Corp.
Joe Hutt - High-Performance Design Tools Manager, IBM Corp.
Kurt Keutzer - Chief Scientist, Synopsys, Inc.
Janusz Rajski - Chief Scientist, Mentor Graphics Corp.
Ronald A. Rohrer - Chief Technologist, Integrated Silicon Systems, Inc.
Larry Rubin - Group V.P., Viewlogic
Jim Solomon - Chief Technologist, Cadence Design Systems, Inc.

PANEL

ARE PARAMETERIZED CORES A SERIOUS BUSINESS?

Moderator: *Daniel D. Gajski* - Univ. of California, Irvine, CA

With 20M transistors/chip available to EVERY system designer in the year 2000, how will they be used? How will complex systems be designed? Microprocessors and a limited number of high volume ICs will still be designed with the same blood, sweat and tears as always. The open question is how we will design the application-specific system?

Some have proposed Application-Specific Integrated Processors (ASIP) as a replacement for ASICs. ASIPs are specialized processors which are customized to each application, including changes to the instruction set, memory interface, etc. to achieve maximum performance. ASIP proponents believe that ASIPs and other parameterizable cores will constitute the basic building blocks of future systems and that the tools industry will supply new system level tools and development environments, including retargetable compilers and run-time systems, to support the design of embedded systems using these programmable cores.

The proponents of an alternate school of thought believe that system tools and environments are difficult to develop and that future systems will be built strictly from standard parts (processors and memories) for which software tools such as standard compilers are readily available on the market.

If either prediction is true, the future looks bleak for the bulk of the EDA industry which lives on the large amount of application specific integrated circuit design for each new system. In the first case, the EDA industry will face the challenge of developing a new set of system design tools, which may be impossible. On the other hand, if the only standard parts (or fixed cores) are used in every application specific system then the EDA industry is selling into a rapidly shrinking market.

This panel will discuss the pros and cons of programmable cores, the core based methodology and its impact on the future of the EDA industry.

Panel Members:

Tadatoshi Ishii - Toshiba Corp., Japan
Bill Lin - IMEC, Belgium
Peter Marwedel - Univ. of Dortmund, Germany
Vijay Nagasamy - LSI Logic, Inc., USA
Pierre Paulin - SGS-Thomson Microelectronics, France

TUTORIAL 1
PRACTICAL ASPECTS OF
FORMAL HARDWARE VERIFICATION

Speakers:

Aarti Gupta, NEC C&C Research Laboratories, Princeton, NJ, *is a researcher in the CAD group, with her main interest in formal methods. She is currently exploring advanced verification techniques for industrial practice.*

Andreas Kuehlmann, IBM Corp., Yorktown Heights, NY, *is project leader in the verification group, where he is involved with formal hardware verification techniques and their practical application for large microprocessor systems.*

Carl Seger, University of British Columbia, Vancouver, BC, *is associate professor of computer science; his main research interests are formal hardware verification and asynchronous circuits. He is the author of the Voss verification system and is co-author of the book "Asynchronous Circuits".*

Background: This tutorial is intended for both CAD developers and tool users interested in practical aspects of formal hardware verification. Attendees should have a basic knowledge of hardware design, functional simulation and modeling.

Description: Verifying the correct behavior of a digital system is becoming an elusive task. Traditional techniques, such as simulation, are often inadequate for covering the large state spaces found in present day processor designs. Formal methods are emerging as a practical solution to specific aspects of the verification problem.

This tutorial will discuss formal hardware verification methods with an emphasis on practical techniques and applications. The tutorial will consist of three parts. First, a historical overview of the hardware verification area will be presented with sufficient background and theory to level-set the audience. Specific topics covered will include underlying concepts from formal logics, automata theory and Boolean function representations as well as the basics of machine equivalence, model checking and language containment.

Next, various aspects of functionally modeling and verifying detailed hardware implementations will be discussed. This part will cover techniques for combinational circuit verification and methods for finite-state machine comparison, including algorithms for state-space exploration and practical approaches for full-chip verification.

Finally, techniques for functional, or high-level verification will be discussed, with emphasis on approaches combining different verification techniques, such as model checking and theorem proving. The discussion will cover both theory and implementation details as well as practical application of these methods. Throughout the tutorial, several non-trivial example circuits and their verification will be discussed.

TUTORIAL 2
HARDWARE/SOFTWARE CODESIGN OF EMBEDDED SYSTEMS

Speakers:

Jörg Henkel, Technische Universität, Braunschweig, Germany, *is a key developer of the pioneering COSYMA system for hardware/software codesign and a leading researcher in this area. He has been involved in the ESPRIT basic research project COBRA for hardware/software codesign.*

Frank Vahid, University of California, Riverside, CA, *is assistant professor of computer science and coauthor of the book "Specification and Design of Embedded Systems". He has been an active researcher in the system design field for over seven years, and had chip design experience at Hewlett-Packard and AMCC.*

Loganath Ramachandran, LSI Logic, Milpitas, CA, *is a senior software engineer in software research and development. Previously he worked as a software engineer in design automation at Texas Instruments.*

Background: This tutorial is intended for researchers, managers, and designers interested in the development of embedded systems comprised of both software and custom digital hardware components. Familiarity with programming languages, hardware description languages, and synthesis will be helpful.

Description: Investigation of the various aspects of hardware/software codesign is a rapidly expanding area. Codesign techniques permit the design of increasingly complex mixed hardware/software systems at a higher level of abstraction than possible with today's tools, and result in a substantial reduction in the economically important time-to-market factor. Furthermore, necessary design techniques such as high-level synthesis have matured to the point where they can be used in industrial environments, making hardware/software codesign techniques feasible.

This tutorial first presents a broad overview of hardware/software codesign. After introducing the economically interesting area of embedded systems, the instructors will describe current approaches to hardware/software codesign, discuss algorithms for the key issue of hardware/software partitioning, and present hardware and software synthesis methods and other topics. The tutorial will demonstrate how hardware/software codesign techniques result in the important effects of short turnaround times, reduced time-to-market, and minimized costs. Finally, the instructors will discuss today's major problems and suggest what is needed for industrial acceptance of hardware/software codesign.

Other areas included will be specification and estimation techniques, different codesign approaches, verification and simulation, and design methodology.

TUTORIAL 3
OPTIMIZATION TECHNIQUES FOR LOW POWER VLSI CIRCUITS

Speakers:

Srinivas Devadas, Massachusetts Institute of Technology, Cambridge, MA, *is associate professor of electrical engineering and computer science. His interests span all aspects of the synthesis of VLSI systems, with recent emphasis on computer aids for the synthesis of low-power electronic circuits.*

Anantha Chandrakasan, Massachusetts Institute of Technology, Cambridge, MA, *is assistant professor of electrical engineering and computer science. He was an architect of the InfoPad low-power wireless terminal, and is a co-author of the book "Low Power CMOS Digital Design".*

Sharad Malik, Princeton University, Princeton, NJ, *is assistant professor of electrical engineering. His research interests are in the synthesis of VLSI circuits, embedded systems design, CAD techniques for low-power circuits, and software-level power analysis and optimization.*

Background: This tutorial is for researchers and practitioners interested in the optimization of VLSI designs for low power. Knowledge of integrated circuit design flow will be helpful.

Description: Power dissipation has become an important parameter in the design of integrated circuits, particularly for portable computers and personal communication systems. This tutorial will describe optimization techniques for low power that can be applied to integrated circuit designs at the circuit, logic, register-transfer, behavioral, system and software levels.

Srinivas Devadas will describe the power dissipation model underlying the optimization methods, and provide background in power estimation. Optimizations to reduce power dissipation at the circuit level will be presented, including transistor reordering and transistor sizing. Transformations to reduce the power dissipation of combinational logic, low-power-driven logic optimization algorithms based on these transformations, and techniques to optimize sequential logic for low power will be described.

Anantha Chandrakasan will present techniques to minimize power consumption at the behavioral and system levels by minimizing power supply voltage and switched capacitance. A key approach combines architecture optimization with voltage scaling; this allows a trade-off between area and power. Algorithmic transformations can be used to significantly reduce power consumption. System-level low-power trade-offs drawn from multimedia portable systems such as the InfoPad will demonstrate that orders of magnitude power reduction are possible.

Since many applications are now implemented as embedded systems (application-specific software running on dedicated processors), power consumption of software also needs to be considered. Sharad Malik will describe techniques for analyzing the power cost of programs and the development of instruction-level power models for some commercial CPUs. Given the ability to evaluate programs in terms of their power/energy costs, it is possible to search the design space in software power optimization. Various techniques for software power optimization will be presented.

TUTORIAL 4
THE SYSTEMATIC DESIGN OF ASYNCHRONOUS CIRCUITS

Speakers*:*

Michael Kishinevsky, University of Aizu, Fukushima, Japan, *is professor in the computer architecture laboratory. He has previously conducted research in St. Petersburgh, Russia, and at the Technical University of Denmark. He is co-author of the books "Concurrent Hardware. The Theory and Practice of Self-Timed Design" and "Self-Timed Control of Concurrent Processes".*

Luciano Lavagno, Politecnico di Torino, Italy, *is assistant professor of electrical engineering. He was previously at the University of California, Berkeley, and has consulted for several design automation companies. He is co-author of the book "Algorithms for Synthesis and Testing of Asynchronous Circuits".*

Peter Vanbekbergen, Synopsys, Inc., Mountain View, CA, *is a member of the technology group and a researcher on asynchronous and low power circuits. He was previously with the Interuniversity Micro Electronics Center (IMEC) in Leuven, Belgium.*

Background: This tutorial will be especially useful to digital circuit designers and design tool developers who want to be informed about the current state of asynchronous designs and design methods.

Description: The purpose of this tutorial is to provide digital circuit designers with an up-to-date overview of existing practical asynchronous design methodologies. It will demonstrate that asynchronous designs are possible now, with techniques that closely match those for synchronous semi-custom and full-custom design.

After an introduction devoted to the explanation of the problem and of the general terminology, the tutorial will briefly describe how the problem of asynchronous circuit design can be tackled, both for data and control units. Concentration will be on the problem of modeling asynchronous circuits, and on the robustness/cost trade-offs involved in choosing (or mixing) delay models.

A detailed description will then be given of an asynchronous design methodology, including specification, state assignment, logic synthesis, and test. A methodology based on a formalized timing diagram-like specification can be applied to the hierarchical design of control circuits with various underlying delay models, and offers good possibilities for CAD support (including semi-custom).

Finally, the tutorial will show how asynchronous design techniques have been applied to the solution of practical problems from a variety of digital areas, from inherently asynchronous busses to advanced high-performance, low-power processing units.

ICCAD-95 REVIEWERS

Emile Aarts
Fred Abramson
Toru Adachi
Jay Adams
Toshio Akino
Charles J. Alpert
Roger Ang
Pranav Ashar
Smita Bakshi
Joe Balardeta
Hakim Bederr
Robert Bencivenga
Narasim Bhat
Sudipta Bhawmik
Kenneth D. Boese
Vamsi Boppana
Daniel Brand
Oliver Bringmann
Stephen Brown
Till Bubeck
Steven Burns
Yang Cai
Pinar Ceyhan
Tapan Chakraborty
Srimat T. Chakradhar
Sreejit Chakravarty
Anantha Chandrakasan
Chwen-Cher Chang
Jau-Shien Chang
Shing-Chong Chang
Louis Chao
Abhijit Chatterjee
Ben Chen
Beyin Chen
D.S. Chen
C. Eric Cheng
David I. Cheng
Scott Chiu
Pai Chou
Laurent Chouraki
Kevin Chung
Sari Coumeri
Florin Dartu
Scott Davidson
Eugene Ding
Nikil Dutt
Gerben Essink
Weiping Fang
Amir Farrahi
Jack Fishburn
Peter Flake
Piero Franco
Robert French
Kent Fuchs
Takashi Fujii
Tetsuro Fujii
Tetsuya Fujimoto
Masahiro Fujita
Kunihiro Fujiyoshi
Uwe Glaeser
Jie Gong
Aarti Gupta
Rohini Gupta
Peter Gutberlet
Dong Sam Ha
Kiyoharu Hamaguchi
Ismed Hartanto
Toshihiro Hattori
Scott Hauck
Ghuya Hayashi
John P. Hayes
Lei He
Jun Hirai
Doug Holberg
Youn-Sik Hong
Tetsuro Honmora
Charles Hough
Ching-Chao Huang
Dennis Jen-Hsin Huang
Jin Huang
Shi-Yu Huang
Yean-Yow Hwang
Hiroshi Ichiryu
Mitsuo Ikeda
Akihiko Inoue
Akio Ishizuka
Masaki Ito
Tomonori Izumi
Sehwoong Jeong
Niraj K. Jha
Pradip Jha
Wen-Ben Jone
Jing-Yang Jou
Eric Juan
Seiji Kajihara
Mineo Kaneko
Kaoru Kawamura
Kei-Yong Khoo
Shinji Kimura
Wim Kloosterhuis
Gernot Koch
Cheng-Kok Koh
Kazuhiro Kohara
Tetsushi Koide
David Kolson
Kevin T. Kornegay
Byron Krauter

ICCAD-95 REVIEWERS

Florian Krohm
Angela Krstic
Andreas Kuehlmann
Chen-Ping Kung
Hiroaki Kunieda
Fadi Kurdahi
William Lam
Chung-Ren Lee
Frank Lee
James Lee
Kuen-Jong Lee
Mike Lee
Terry Lee
James Lewandowski
Hsing-Chung Liang
Wentoh Liao
Chih-Jen Lin
Weiliang Lin
Paul Lippens
Huan Liu
Paul Sheng-Chun Lo
David Long
Philip Lopresti
Marcelo Lubaszewski
Patrick M. Madden
Jean Christophe Madre
Frederic Mailhot
Masato Maruyama
Meyriem Marzouki
Karti Mayaram
Edward J. McCluskey
Noel Menezes
Shin-ichi Minato
Salvador Mir
Takashi Mitsuhashi
Hiroshi Miyashita
Toshiaki Miyazaki
Fiar Mohamed
Sundararajarao Mohan
Byung-Ro Moon
Sudhakar Muddu
Fidel Muradali
Hiroshi Murata
Paul Murphy
Sudip Nag
Akito Nagatsu
Akira Nagoya
Hiroshi Nakamura
Yuichi Nakamura
Yukihiro Nakamura
Takeshi Nakamura
Shigetoshi Nakatake
Michel Nicolaidis
Cees Niessen
Mitsuru Nomura
Masahiro Numa
Richard O’Connor
Yasushi Ogawa
Kiyashi Oguri
Seong Ohm
Yasushi Okada
Alex Orailoglu
Ross Ortega
Chen-Yang Pan
Peichen Pan
Preeti Panda
Janak Patel
Srinivas Patil
Ad Peeters
Irith Pomeranz
Dave Pursley
Chen Guang Qiu
Katarzyna Radecka
Salil Raje
Venky Ramachandran
D. Sreenivasa Rao
Jeff Rearick
Michel Renovell
Min-Joong Rim
Rob Roy
Jaijeet Roychowdhury
Toshiyuki Sadakane
Hidenori Sato
Masao Sato
Hiroshi Sawada
Prashant Sawkar
William J. Schilp
Herman Schmit
Endric Schubert
Eva Schubert
Lu Sha
Satoshi Shibatani
Takashi Shimamoto
Youichi Shiraishi
Kazuhiro Shirakawa
Toshio Shoji
James Sienicki
Mani Soma
Larry Soule
William W. Stiehl
Leon Stok
Chauchin Su
Wern-Jieh Sun
Kei Suzuki
Atsushi Takahara
Atsushi Takahashi
Kazuhiro Takahashi
Kazuhiko Takamizawa

ICCAD-95 REVIEWERS

Yasuhiro Takashima
Kazuo Tamakashi
Nagesh Tamarapalli
Masaaki Tanabe
Gustavo Tellez
Masayuki Terai
Tsuneo Tomita
Hiroyuki Tomiyama
Nur Touba
Masahiko Toyonaga
Christoph Trautwein
ChungWen Albert Tsao
Nobuo Tsuda
Shuuji Tsukiyama
Akihiro Tsutsui
Bogdan Tutuianu
C.A.J. van Eijk
Jef van Meerbergen
Srikanth Venkataraman
Ashok Vittal
Arthur de Vries
Shin-ichi Wakabayashi
Hong-Mo Wang
Joe Wang
Kenji Watanabe
Tshimasa Watanabe
Christoph Weiler
Uli Weinmann
Jen Pin Weng
Alan Westwick
John Willis
Martin Wong
Chen-Wen Wu
Wen-Chien Wu
Xun Xiong
Dongmin Xu
Min Xu
Takayuki Yamanouchi
Masahide Yamashita
Chung-Do Yang
Honghua Yang
Fu-Ming Yeh
Thomas Yin
Chang-Sheng Ying
Goichi Yokomizo
Takeshi Yoshimura
Chiyoshi Yoshioka
Qisui Zhang
Zeljko Zilic