This paper studies the importance of the different contributions to the power of telecom ASICs, comparing results for 0.5u and 0.7u designs. As a result, library development, in particular for RAMs, is identified as a key challenge to obtain low-power ASICs.

1. Introduction

Recently, the cooling problems of state-of-the-art ICs and the boom of battery-operated electronics have caused a large interest in power-reduction techniques. In the literature, the main focus is the reduction of the \( fC \)-product of the outputs of the logic gates, where \( f \) is the product of the clock period and the probability of having a rising transition at the node, and \( C \) its load capacitance.

In contrast, our approach was to start with an analysis of the relative importance of the different contributions (logic gates, clock, RAM, I/O). In the past, we carried out such an analysis for a set of 0.7u ICs that was designed at Alcatel–Bell. Surprisingly, it appeared that the most important contribution was due to the clock circuitry inside the flip-flops. As a result, we developed a synchronous gated-clock strategy that enabled an impressive power reduction, while retaining the easiness and safety of synchronous design [3].

However, the ratios between the different contributions can shift from one technology generation to another. Therefore, they must be re-evaluated on a regular basis. This paper presents data for 0.5u designs and compares the importance of the different contributions with the data for 0.7u designs.

2. Power contributions: importance

We distinguish the following contributions:

- clock power: due to the clock drivers, the clocknet routing, and the input capacitances of the flip-flops.
- clockInFF power: due to the circuitry inside the flip-flops that switches when the flip-flop is clocked even if its output remains constant.
- I/O power.
- power dissipated internally in the standard-cells.
- intercell C power: due to the interconnect capacitances and the input capacitances of the cells.
- RAM power.

Figures 1 and 2 show the contributions to the power for a typical recent Alcatel–Bell design, which measures 60mm² in a 0.5u technology. Figure 1 shows the results for a 0.7u implementation, operating at a supply voltage of 5V. Figure 2 shows the results for a 0.5u implementation, operating at a supply voltage of 3.3V.
The considered device contained 13 RAMs, corresponding to an area of 16mm² in the 0.5μ technology. The device was actually processed in 0.5μ. The 0.7μ data are shown only to illustrate the power-consumption trends.

Two clear trends can be observed:

- the power is dominated by the RAM power.
- the remaining power is for a large fraction related to the clocking of the circuit.

These trends are discussed in the next two sections.

3. RAM power

A telecom ASIC is typically processing a dataflow, as shown in Figure 3. RAM is present mainly for 2 purposes:

- store status information for the processing blocks.
- acts as data buffers between the processing blocks.

As a result, a telecom ASIC often contains a lot of relatively small RAMs.

![Figure 3. Telecom ASIC structure](image)

As illustrated in figures 1 and 2, our experiments lead to the conclusion that in a 0.5μ telecom ASIC, the RAM power has become the dominating power contribution. This is due to 2 factors:

- The high density of a 0.5μ technology allows to implement complete systems on a single chip, integrating in particular large amounts of RAMs on-chip. In the past, only small RAMs were implemented on-chip. Medium and large-size RAMs were implemented using standard components. At that time, the RAM power figures were characteristics of standard components. In contrast, they have now become very important characteristics of a silicon technology (and library offering). In fact, the contribution of the RAM to the power of the 0.7μ implementation of the 0.5μ device considered in Figures 1 and 2 is significantly higher than the contribution of the RAM we observed in real 0.7μ ASICs that were designed in the past at Alcatel-Bell.
- RAM-power does not scale as easily with technology improvements as the other contributions do.

For the other contributions to the power consumption, the scaling is almost straightforward from the scaling of the voltage and the linear dimensions. Library development for RAMs, on the other hand, represents a major challenge. It is complicated by the fact that a RAM has a number of different quality measures: power, access-time, density,... and the fact that the relation between these quality measures is much more complex than for standard cells.

This is illustrated in Figure 4, which compares the 2kx16 single-port RAM offerings of 3 Si-vendors (0.5μ technology).

![Figure 4. Characteristics of 2kx16 sp–RAMs](image)

For small RAMs, the differences in power are even more pronounced, as shown in Figure 5.

![Figure 5. Characteristics of 32x8 sp–RAMs](image)

Consensus is growing among RAM developers to use different RAM-generators for small and large RAMs, because the use of a single generator will particularly for
small RAMs lead to an overdimensioning of the drive capabilities and thus to a waste of power.

In addition, research is ongoing at IMEC and Alcatel-Bell to minimize e.g. the number of memory accesses by algorithmic and architectural modifications [1, 2].

4. Power due to clocking

The second major power contribution is due to the clocking of the circuit. Particularly in telecom ASICs, this contribution is large with respect to the power of the combinational logic, because only a fraction of the logic is active every cycle of the clock period. The remainder of the logic is only active for a few cycles per data-frame of x-bytes, or when a specific error condition occurs, or when the on-board controller issues a command to the ASIC.

Directions to reduce the clock-related power are:

- activate a block only when it is needed, and at that moment clock it at the minimum possible clock frequency.
- use clocktree synthesis to minimize the clock-routing capacitance.
- limit the power due to the nodes inside the flip-flops that are as active as the clock (cf. Figure 6). this can be done using a synchronous gated-clock strategy [3] or by a clever library development that reduces the capacitances that are as active as the clock.

Figure 6. Clock circuitry inside a traditional flip-flop.

5. Bibliography

