

Fault Modeling of Differential ECL

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Abstract

The paper deals with testability analysis of differential ECL. The logic behaviour and the drop in performance concerning a very detailed list of possible defects of a high speed ECL-Design was examined. The testcircuit, an AND gate (bandwidth: dc to 3.4 Gb/s), was designed taking into account a low power consumption and a small overhead as it is used for weighted random pattern generation and signature analysis (edge counting) within a Built-In-Self-Test (BIST)-Architecture. It was realized using a 1.2 μm bipolar technology. It will be shown that defects in differential ECL devices may cause redundant or delay faults in respect to operation speed.

1. Introduction

Non-saturated logic like ECL (Emitter Coupled Logic) or CML (Current Mode Logic), a simplified version of ECL in which emitter followers are omitted, is most suitable for designing high-speed integrated circuits. The fact that in normal mode of operation none of the transistors saturates, leads to short gate delays of far below 1 ns and bit rates up to 40 Gb/s [1]. Subnanosecond-gate delays are required for e.g. [2]:

- supercomputers
- mainframe-computers
- graphic-processors
- optical transmission systems
- measurement technology
- real-time image-processing

Until now, no publication about fault modeling of wide-band (high speed) differential ECL or E²CL could be found. Most papers deal with fault modeling or testability analysis of CMOS [3] [4] [5], BICMOS [6] [4] [7] [8] or TTL [3] [9] [10] circuits. [11] and [4] are the

first investigating a standard single-ended ECL OR/NOR gate.

Hence, the performance and the behaviour of the AND gate under a set of defects were examined in order to get general information about defective differential ECL or E²CL circuits.

2. High Speed Bipolar ECL-Circuits

A problem of high speed (and consequently of wide-band) circuits is that a decreasing gate delay causes an increasing power dissipation.

$$td \sim \frac{V_0 \Delta V C_{\text{eff}}}{P} \quad (1)$$

(td: delay time, P: power dissipation, V₀: supply voltage, ΔV : voltage swing, C_{eff}: effective junction and interconnect capacitances)

As shown in (1) a short switching time and a low power dissipation are obviously contradictory requirements because decreasing the power dissipation implies decreasing the currents available for charge variations of parasitic capacitances [12]. A low power dissipation can be obtained by using a low (output) voltage swing that allows V₀ to decrease as well. Besides, operating the transistors with a small V_{CE} (collector-emitter voltage), which means operating near the high-current or quasi-saturation region, decreases P.

Only if suitable circuit concepts (full custom designs) are chosen and the circuits themselves are carefully optimized, can high operating speed be achieved. A careful and individual design of transistors leads to a compromise between demands for low base spreading resistance and low junction capacitance. Standard circuits are not appropriate for most requirements. Therefore, a full custom monolithic integrated AND gate, as shown in Fig. 1, was designed using the so-called series gating principle (current switches are stacked so that several signal levels are obtained). It is part of a

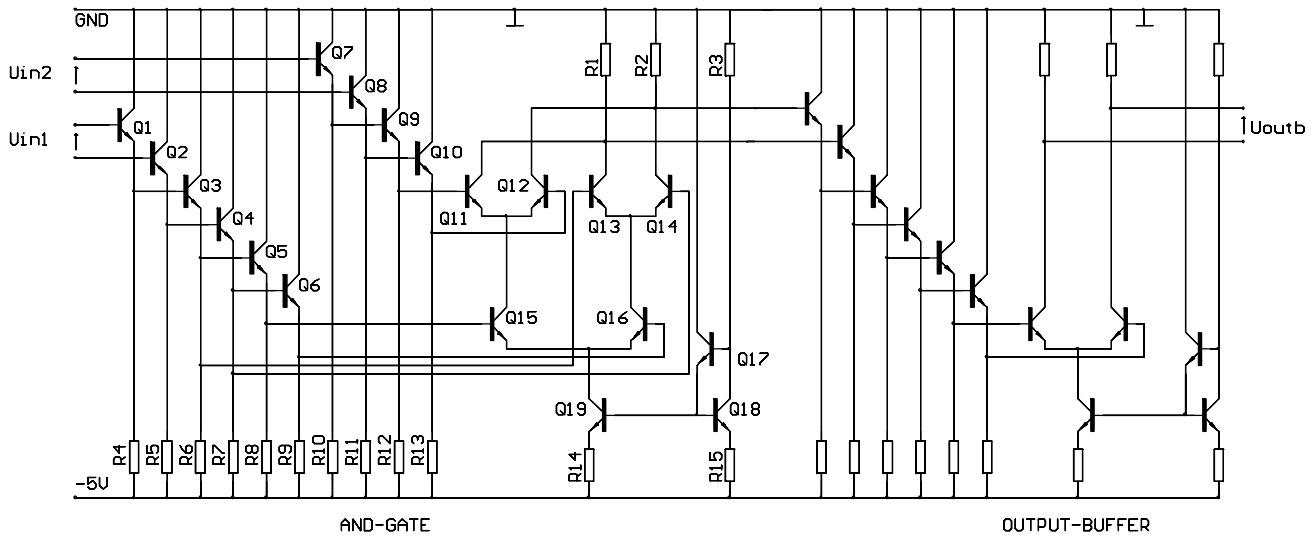


Fig. 1: Test-Circuit

BIST-architecture and especially designed for the use in weighted random pattern generators and for test response analysis (edge counting). The AND gate consists of two stacked levels of emitter coupled differential transistor pairs called current-switches. The lower level consists of a single transistor pair which drives the cross-coupled pairs of the upper level. One data-input drives the upper current switch level by two emitter-follower pairs. The other data-input drives the lower level by three emitter-follower pairs. The symmetry of the AND gate in respect to the output makes it superior to the standard ECL AND gate [13] in several applications. An output-buffer is used in order to reduce spikes on the output signal which occur if input signals change simultaneously. Using 50 Ω loads, the output voltage swing of this buffer is:

$$\Delta V_{out} = 400 \text{ mV}_{pp}.$$

The AND gate is designed using "differential logic". Reference inputs as common in single-ended techniques are used as additional inputs in order to drive current switches by differential signals. In comparison with single-ended ECL, differential ECL has several advantages. The voltage swing is halved, which decreases the power dissipation (1). The shape of pulse-edges becomes improved and symmetrical. Time-jitter and crosstalking are reduced.

Because of the small voltage swing using small loads (typ. 50 Ω), the switching time becomes shorter.

3. Analysis of physical defects

Fault models are a description of the changed behaviour of a circuit as a result of a defect or failure.

Thus, a useful fault model will naturally lead to a test generation procedure for the fault [3]. Defects and failures in ECL can be abstracted to shorts and opens in interconnects and in open connections, shorts between device terminals and in emitter-collector pipes of bipolar devices. The following possible defects of ECL were investigated:

- emitter open
- collector open
- base open
- emitter-collector pipe
- emitter-collector short
- emitter-base short
- collector-base short
- resistor short
- resistor open
- shorts of interconnects

A short between interconnects (two lines) was modeled as a non-resistive connection. An open was taken into account as a large resistor (1 G Ω) inserted between the two nodes. A small capacitor of 0.001 pF, that is sometimes used in parallel to this resistor [4], did not have any effect on the results of the simulations and was therefore omitted.

Collector-emitter pipes are used within a range from 400 Ω to 4.7 K Ω [4] [6] [11]. Here a pipe was modeled as a 1 K Ω resistor between emitter and collector of the respective transistor.

Although the number of possible defects and faults becomes larger with an increasing complexity of ICs, it is first of all necessary to investigate the behaviour of the test-circuit at the transistor level, particularly as fault

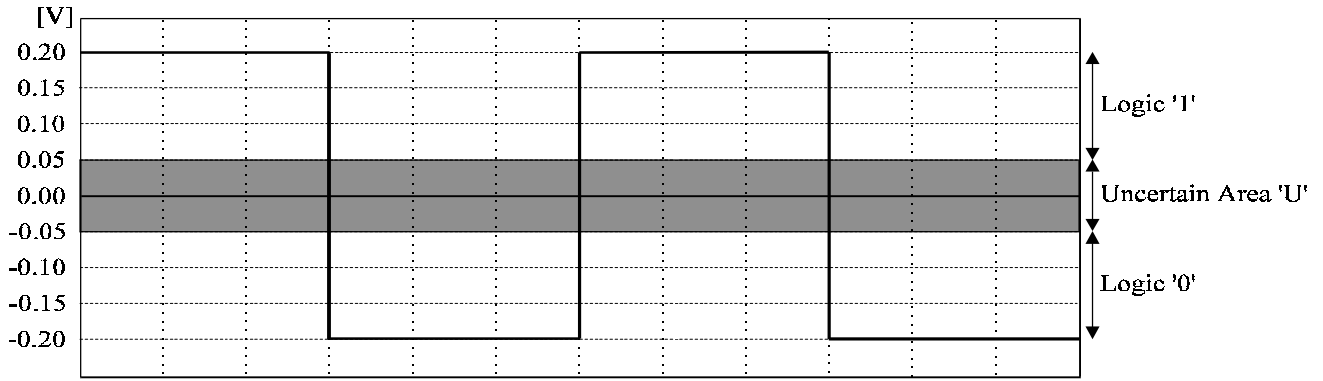


Fig. 2: Level-definition

models at the transistor level can characterize physical failures quite accurately [3]. Furthermore, this facilitates the development of fault models for higher levels such as gate-level, interconnect- or device-level.

The AND gate was simulated using SPICE and ELDO. There was only one defect modeled at a time. A number of 173 possible defects altogether have been taken into account. An output buffer regenerates a logic '1' with an output voltage of the AND gate within an interval from 50 mV to 200 mV and a logic '0' within an interval from -200 mV to -50 mV (Fig. 2.). Output voltages within the uncertain area (-50 mV to 50 mV)

can not be regenerated by the buffer over the whole bandwidth (and lead to a fault).

As specific definitions of pulse transition and propagation delay times are needed for a description of the dynamic characteristics of the AND gate, delays, rise and falltime are measured as shown in Fig. 3. Rise and falltimes t_r and t_f are defined between the 10% and 90% points of the total voltage transition.

The total voltage range of input and output here is taken to be V_{OL} to V_{OH} . Propagation delay times from input to output, denoted t_{PHL} and t_{PLH} , are defined between the 50% points of the input and output pulse waveforms [14].

4. DC-Test

First, the stuck-at fault model was used. It was found out (by a DC-simulation) that several defects can not be detected by a DC-Test. Only 134 of the 173 (77.5%) investigated defects are detectable. The detected faults were subdivided into 13 fault-groups (fg).

Table 1 lists the various fault-groups. Using collector-emitter pipes with rather low values of 400 Ω some more defects become detectable as shown below in table 2.

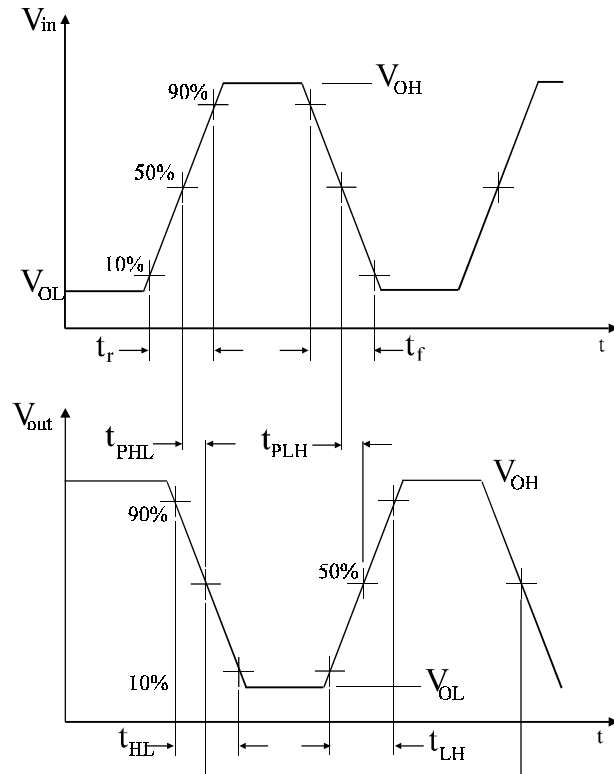


Fig. 3: Definition of transition and delay times

Table 2: Additional faults using 400 Ω -pipe

Transistor	From Fault-Group	To Fault-Group
Q1cep	ff	fg2
Q2cep	ff	fg1
Q7cep	ff	fg3
Q8cep	ff	fg1
Q18cep	ff	fg6

cep = collector-emitter pipe

In table 3 the behaviour of the AND gate in consideration on the various fault-groups is listed. As it can be seen, the fault-groups fg5, fg6, fg7, fg8, fg9, fg11, fg12 and fg13 lead to an undefined logic level ('U').

Table 1: Fault-groups and corresponding defects

fg	corresponding defect
ff	Q1/Q2/Q3/Q4/Q5/Q6/Q7/Q8/Q9/Q10/Q13/Q17 co, Q13 eo/bo, R4/R5/R6/R7/R8/R9/R10/R12 o, Q1/Q2/Q7/Q8/Q18/Q19 bcs, Q17 bes, Q14/Q19 ces, Q1/Q2/Q7/Q8/Q14/Q17/Q18/Q19 cep
fg1	Q11 co, Q1/Q3/Q7/Q9/Q11 bo, Q1/Q3/Q7/Q9/Q11 eo, R2/R13 o, Q4/Q6/Q10/Q12/Q14 bcs, Q2/Q4/Q8/Q10 bes, Q2/Q4/Q8/Q10/Q12 ces, R4/R6/R8/R10/R12 s, Q4/Q10/Q12 cep
fg2	Q2/Q4/Q6/Q16 bo, Q2/Q4/Q6/Q16 eo, Q3 bcs, Q1/Q3/Q5 bes, Q1/Q15 ces, R5/R7/R9 s, (R4/R5)/(R5/R6)/(R6/R7)/(R7/R8) bf, Q3/Q5 cep
fg3	Q12/Q15 co, Q5/Q8/Q10/Q12/Q15 bo, Q5/Q8/Q10/Q12/Q15 eo, Q9/Q11 bcs, Q6/Q7/Q9 bes, Q7/Q9/Q11/Q16 ces, R11/R13 s, (R11/R12) bf, Q6/Q9/Q11 cep
fg4	Q14 co/bo/eo, Q13 ces, Q13 cep
fg5	Q15 bcs, Q15 cep
fg6	Q18/Q19 co, Q17/Q18/Q19 bo, Q17/Q18/Q19 eo, R3/R14/R15 o, Q5/Q17 bcs, Q15/Q16/Q18/Q19 bes, Q3/Q5/Q6/Q17/Q18 ces, R3/R15 s, (R9/R10)/(R1/R2) bf
fg7	Q16 co, Q13/Q14 bes
fg8	Q16 bcs, Q16 cep
fg9	Q11/Q12 bes, (R10/R11)/(R12/R13) bf
fg10	R1 o, Q13 bcs
fg11	(R8/R9) bf
fg12	R11 o, R1 s
fg13	R2/R14 s

ff = faultfree, fg = fault-group,
o = open, s = short, co = collector open,
eo = emitter open, bo = base open,
bf = bridging fault, bcs = base-collector short,
bes = base-emitter short, ces = collector-emitter short,
cep = collector-emitter pipe

5. Dynamic-Test

All 173 defects were modeled using input signals with frequencies varying from 0.1 GHz to 1.7 GHz (maximum input-frequency). Simulations are made at 0.1 GHz, 0.25 GHz, 0.5 GHz, 1.0 GHz, 1.1 GHz, 1.5 GHz and 1.7 GHz. All possible combinations of input signals were applied to the AND gate. The results of this simulation are shown in Fig. 4. The number of detectable defects

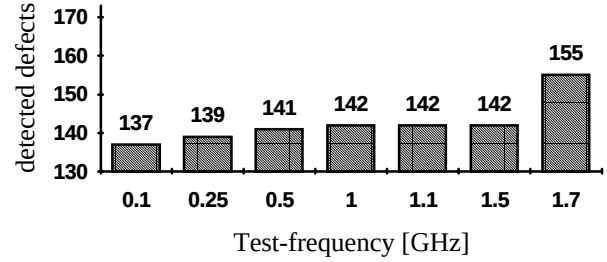


Fig. 4: AC-Test

goes up with increasing test-frequencies. Only 18 defects are not detectable at the maximum input frequency of 1.7 GHz. Especially open collectors and base-collector shorts of emitter followers lead to redundant faults at lower input frequencies.

The input stage of the AND gate consists of emitter follower pairs, which are required for level shifting and impedance transformation. The input impedance is high so that the circuit imposes little loading on the driving signal. Large currents can be driven into external resistive or capacitive loads by the low output impedance.

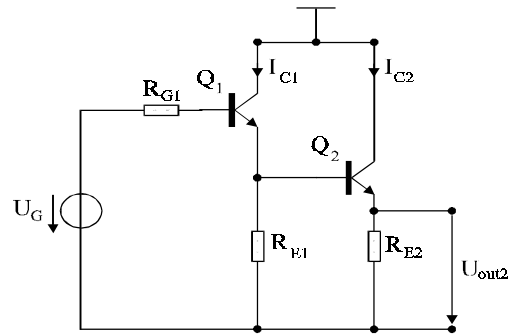


Fig. 5: Emitter follower input stage

An emitter follower with an open collector as well as with a base-collector short works as a diode, but with different transient behaviour. Therefore, it is also useful for level shifting, but is inferior to the transient behaviour of a non defective emitter follower. The output impedance of an input stage (3) consisting of two emitter

Table 3: ECL AND Gate: Stuck Open/Short Analysis

input	ff	fg1	fg2	fg3	fg4	fg5	fg6	fg7	fg8	fg9	fg10	fg11	fg12	fg13
A B	Q	Q	Q	Q	Q	Q	Q	Q	Q	Q	Q	Q	Q	Q
0 0	0	0	0	0	1	0	U	U	0	0	1	0	0	U
1 0	0	0	1	0	1	U	U	U	0	0	1	U	0	U
0 1	0	0	0	1	0	0	U	0	U	U	1	U	0	U
1 1	1	0	1	1	1	1	U	1	1	U	1	1	U	1

Q = output signal ; A, B = input signal ; ff = faultfree

followers (as shown in Fig. 5.) is up to 50% lower than that using a diode (5) instead of a transistor.

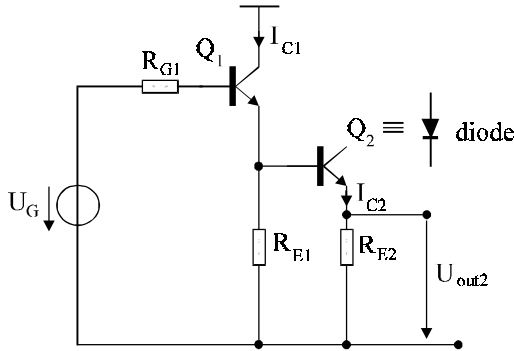
The output impedance of the first stage is:

$$R_{out1} = \left(\frac{U_T}{I_{C1}} + \frac{R_{G1} + r_{b1}}{\beta_1} \right) \parallel R_{E1} \quad (2)$$

The output impedance of the second stage is:

$$R_{out2} = \left(\frac{U_T}{I_{C2}} + \frac{R_{out1} + r_{b2}}{\beta_2} \right) \parallel R_{E2} \quad (3)$$

β : dynamic current gain
 U_T : thermal voltage
 r_b : base resistance

**Fig. 6: Emitter follower-diode input stage**

The variable r_d corresponds to the diode impedance for the static case [13]:

$$r_d = r_e + \frac{r_b}{B_N + 1} \quad (4)$$

B_N : static current gain
 r_e : emitter resistance

Therefore, the output impedance of the second stage is:

$$R_{out2} = R_{out1} + r_d \quad (5)$$

The different transient behaviour is detectable at the maximum input frequency of 1.7 GHz in most cases. Otherwise a delay test may detect such defects.

6. Delay-Test

In order to find out the effects of the 18 non-detectable defects, the gate delays of the CUT (Circuit Under Test) which depend on these defects were simulated and measured at the maximum input frequency. A gate delay of 132 ps was measured for the faultfree (non-defective) AND gate. With this method, another 14 defects can be detected as shown in table 4.

Only 4 defects (base-collector short of the first emitter follower pairs of both inputs) are not detectable at all with the used simulation-environment. They lead to redundant faults.

But using the CUT with base-collector shorts of the first emitter follower pairs within a system leads to a fault as the outputs of a circuit driving the CUT are shorted to ground (GND).

Table 4: Delays corresponding to defects

defect	gate delay difference
ff	0.0 %
Q1/Q2/Q7/Q8 base-collector short	0.0 %
Q7/Q9/Q17 collector open	31.8 %
Q2/Q8 pipe	9.8 %
Q13 collector open	6.8 %
Q13 emitter/base open	1.5 %
Q14 pipe	5.1 %
Q17 pipe	25.8 %
Q17 base-emitter short	3.8 %
Q18 base-collector short	3.8 %
Q19 pipe	5.3 %
Q19 base collector short	17.4 %

ff = faultfree

Every testpattern, followed by every possible testpattern, and longer periods of the same testpattern were applied to the testcircuit. It has been taken into account, as known from CMOS, that it may be important by which testpattern the actual pattern is followed. As expected especially fast switching transitions enable the detection of faults.

7. Conclusion

A differential AND gate under a set of 173 different defects was investigated in order to get general information about defective differential ECL or E²CL circuits. Defects in ECL devices that cause open collectors or base-collector shorts of emitter followers may not be detectable with an AC-test, as they lead to redundant faults. It is shown in the paper that a delay test in addition to a DC-test and an AC-test facilitates a rather high fault coverage.

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