Session 11C: IDDQ Testing

Moderators:

C. Hawkins, University of New Mexico, USA and
K. Baker, Philips Research Laboratories, The Netherlands

In this Session the design problems of IDDQ sensors are covered and also the automatic synthesis of current testable circuits is addressed.

Correlation Between $I_{\text{IDDQ}}$ Testing Quality and Sensor Accuracy
M. Dalpasso, M. Favalli, and P. Olivo

Synthesis of $I_{\text{IDDQ}}$-Testable Circuits: Integrating Built-in Current Sensors
H.-J. Wunderlich, M. Herzog, J. Figueras, J. Carrasco, and A. Calderón

A Built-in Quiescent Current Monitor for CMOS VLSI Circuits