Session 10C: Delay Testing and Diagnosis
Moderators:
T. Vierhaus, GMD, Germany and
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The Netherlands

This Session deals with new algorithms for exact computation of path
delay fault coverage for large combinational circuits as well as robust
and non-robust test pattern generation. Problems of diagnosis of delay
faults in synchronous sequential circuits are also addressed.

An Efficient Method for Computing Exact Path Delay Fault Coverage
B. Kapoor

BIT Parallel Test Pattern Generation for Path Delay Faults
M. Henftling and H. Wittmann

A Trace-Based Method for Delay Fault Diagnosis in Synchronous Sequential Circuits
P. Girard, C. Landrault, S. Pravossoudovitch, and B. Rodriguez