Session 10A: Hierarchical Layout
Moderators:
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This Session addresses hierarchical methods in layout synthesis. The first paper describes the influence of restricted pin positions on the cell area during top-down chip planning. The other two papers focus on EMC-driven midway routing and on hierarchical multi-layer global routing combining top-down and bottom-up routers.

The Effect of Pin Constraints on Layout Area
B. Schürmann and J. Altmeyer

EMC-Driven Midway Routing On PCBs
H. Schmidt, D. Theune, R. Thiele, and T. Lengauer

A Hybrid Hierarchical Approach for Multi-Layer Global Routing
M. Hayashi and S. Tsukiyama